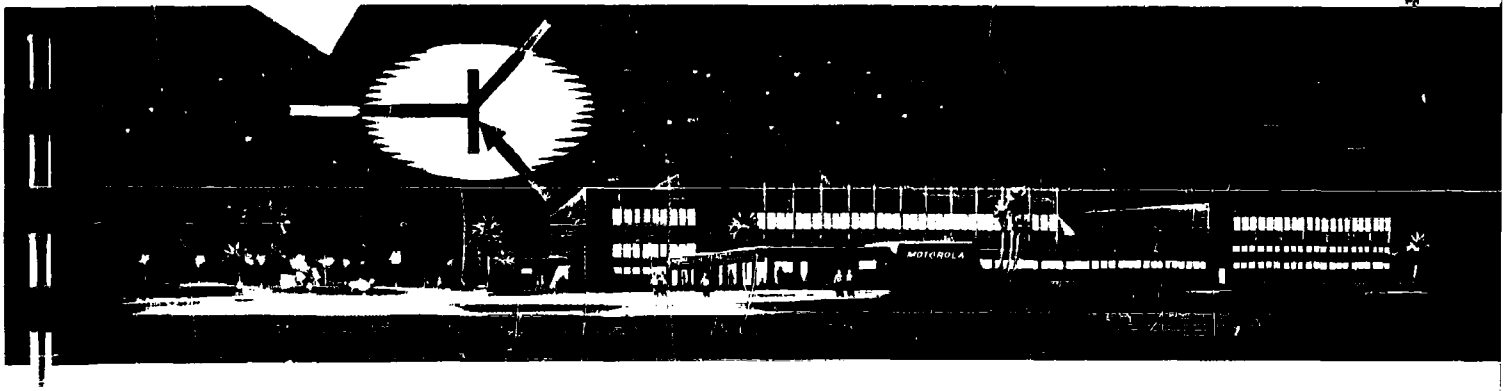
SECOND QUARTERLY REPORT
COMPATIBLE TECHNIQUES
FOR
INTEGRATED CIRCUITRY

U. S. AIR FORCE
CONTRACT NO. AF33(616)8276

Period Covered
1 August 1961 to 31 October 1961

prepared for

U. S. AIR FORCE
AERONAUTICAL SYSTEMS DIVISION
WRIGHT-PATTERSON AIR FORCE BASE, OHIO



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SECOND QUARTERLY REPORT

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Prepared by....

MOTOROLA INC.
SEMICONDUCTOR PRODUCTS DIVISION
PHOENIX, ARIZONA

December 1, 1961

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1.0 INTRODUCTION

This report covers the second quarter's efforts in developing Compatible Techniques For Integrated Circuitry on contract AF 33(616)-8276.

Most of the effort to date has been spent in developing process techniques which are necessary for Integrated Circuit fabrication. This effort has been both in morphological areas and thin films as applied to semiconducting substrate.

Further efforts in perfecting our epitaxial techniques are reported. A program has been started to develop and fabricate typical circuits which are practical for a wide range of high and low frequency amplifier applications as well as logic circuits.

2.0 PROCESS DEVELOPMENT AND PROCESS COMPATABILITY

2.1 EPITAXIAL GROWTH

2.1.1 Closed Tube Epitaxial Gallium Arsenide

Attempts have continued to obtain smooth deposits of GaAs on geranium substrates in the closed tube process. Since earlier attempts had resulted in terraced and pyramided surfaces, it was decided to vary the gas pressure between 64 mm of Hg at 30°C and 2 mm of Hg HCl in an attempt to reduce the growth rate and move closely approach equilibrim. With pressures below 10 mm, extremely small growth rates were observed. A pressure of 10 mm yielded reasonable growth rate but did not resolve the pyramidal growth problem.

With the pressure of HCl stabilized at about 10 mm of Hg, both source and substrate temperatures were raised in order to give the deposition GaAs more energy upon reaching the substrate, and, hence, more surface mobility. The source GaAs temperature was raised to approximately 850°C and a temperature drop of 15° to 30°C between the source and the substrate was maintained. At these elevated temperatures, thermal gradiants became critical and resulted in areas of polycrystalline growth, or even no growth at all. In areas where planar growth did occur a definite improvement in the surface was noted and pyramiding had virtually disappeared, but the presence

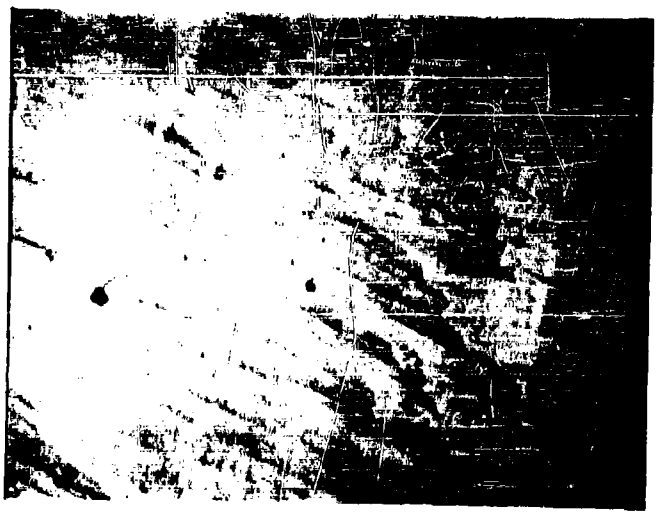
of thermal gradients produced the uneven surface illustrated in Figure 2.1.

Over several runs made under the above conditions some depositions were entirely polycrystalline although all independent variables were maintained as constant as possible. In no case was good planar growth obtained.

In the belief that the poor planar growth might be the result of contamination in the vacuum system and in the HCl lines, the system was dismantled, cleaned and partially redesigned to allow flushing of the HCl lines prior to charging the ampoule. This resulted in an immediate improvement in the growth habit. Single crystal growth was obtainable even with HCl pressures as high as 30 mm of Hg which permitted a faster growth rate than available at a 10 mm pressure with no deterioration of surface quality. The problem of thermal gradients still remained, however, as evidenced by thickness variations across the wafer and by the pattern of the surface features.

In an effort to further reduce the thermal gradients across the wafer, the ampoule design was altered to give a large flat region to support the substrate. It was hoped that the improved contact between the substrate and the quartz, and the quartz and copper heat sink would produce beneficial results.

Two subsequent runs resulted in single crystal growth with



33 X

EPITAXIAL Ga As DEPOSITED
AT 830° C

FIGURE 2.1

surfaces of reasonably good quality. No pyramids were observed although the surface showed a snow-drifting effect. See Figure 2.2.

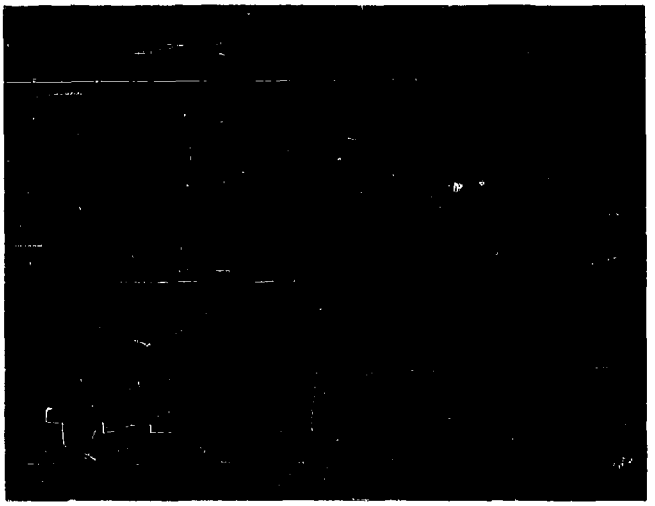
These substrates were deposited from a source held at approximately 850°C with a 15° to 30°C gradient between source and substrate. Hydrogen chloride pressure was 30 mm of Hg at room temperature. Further design improvements are underway in the vacuum and gas charging apparatus. It has been found necessary to adequately protect the vacuum pump from HCl and to improve control of the gas charging system.

Beveling and staining techniques performed on a single crystal deposits grown on several P-type germanium substrates have revealed two bands of material at the GaAs-Ge interface. (See Figure 2.3). These light bands appear on substrates held at temperatures around 800°C or above. They measure one to two microns thick and are as yet unidentified. The possibility exists that at these temperatures, new phases are forming by reaction of GaAs with germanium.

Work is continuing on a short vertical crucible type furnace to replace the present horizontal tube furnace. It is hoped that a proper gradient can be maintained in this type of furnace without the use of a heat sink.

2.1.2. Open Tube Epitaxial Gallium Arsenide

A horizontal two zone, resistance heated furnace has been



SINGLE CRYSTAL GALLIUM ARSENIDE

FIGURE 2.2

EPITAXIAL GaAs ON Ge

FIGURE 2.3

assembled and auxiliary gas control equipment installed. In this furnace HCl gas is metered and mixed with a metered amount of hydrogen and flowed down a quartz tube. The gas passes over granular GaAs then over several geranium substrates at a lower temperature. Deposites of GaAs have taken place in nearly every attempt, but general quality of early runs was poor. Most runs resulted in polycrystallic growth. The presence of dendrites and whiskers deposited on the germanium boat and heave deposition on the tube walls indicate a very high reaction and deposition rate. The heavy whisker grown in the open tube operation was eliminated by lowering the HCl flow rate through the steep thermal gradient in the deposition region. However, growth on the substrate remained polycrystalline.

The former two zone furnace was then replaced by a single zone pre-heater and a three-zone deposition furnace. With three zones of control in the deposition area a flat thermal gradient could be maintained over the substrate wafers. Proper control of this is expected to allow identical deposition to occur upon several substrates simultaneously. In addition, a commercial gas purifier was installed in the hydrogen system. Tests revealed that the gas was relatively clean and the system is periodically checked for leaks.

Experiments now underway are designed to determine the optimum temperature, pressure and flow rate.

The GaAs source is held at approximately 900°C. Early experiments showed that the highest temperature at which deposition occurred was approximately 680°C on the furnace profile. Subsequent experiments revealed that raising the maxium deposition temperature, and designing the GaAs source boat to produce a more efficient reaction between HCl and GaAs apparently raised the partial pressure sufficiently to bring deposition up to 800°C. However, at this temperature, much of the deposition is still polycrystalline and further work is under way to assure a proper HCl concentration, and that the substrate temperatures of the gas stream above them are approximately equal.

2.1.3 Characterization of Epitaxial Material

At the beginning of this reporting period, the primary area of investigation was that of epitaxial layer analyses and diffusion. In this area;

1. Investigations were made to determine variations in resistivity as a function of thickness.

2. Methods for beveling and staining epitaxial layers were developed.

3. Diffusions in epitaxial layers were made and analyzed.

4. Circuit patterns were constructed and diffused structures were analyzed.

5. New methods of gas etching were evaluated and the results showed that;

a. The resultant surfaces are quite good for small amounts of silicon removed at slow etch rates;

b. Quality of the surface varies inversely with the etch rate and the amount of silicon removed;

c. A grown oxide protects against etching.

Additional time during the past period was spent in finishing the evaluation of stainless steel containers for trichlorosilane and silicon tetrachloride; completing the evaluation of a new metal dope injection system; evaluating reaction mechanism more fully in the epitaxial process; and beginning studies on the vapor phase etching of silicon with hydrogen chloride gas.

As reported previously, the use of stainless steel containers for trichlorosilane storage was being evaluated. It has been found that grown layers from trichlorosilane stored in stainless are greater than 10 OHM-CM. Resistivitiesof fr. 10 to 500 OHM-CM have been measured (4 point probe). The resistivity obtained depended on the

growth conditions and substrate used. Silicon tetrachloride stored in stainless steel also gave resistivities above 10 OHM-CM. Stainless steel appears to be a much better storage vessel for trichlorosilane than pyrex.

A new dope injection system using all metal tubing was built as previously reported and doping to the 5 OHM-CM leven was achieved. This system has given excellent control of resistivity in the range up to about 1 OHM-CM, and further investigations are being conducted at higher resistivities.

Some time was spent studying the reaction mechanism of the deposition process. Helium was substituted for hydrogen as a carrier gas for the trichlorosilane, and no silicon deposition occurred. This result shows that silicon deposition involves the reaction of hydrogen with trichlorosilane and that hydrogen chloride gas is formed.

Another experiment was conducted to investigate the possibility of a reverse reaction. Hydrogen chloride gas carried by hydrogen was passed through the reaction tube in a manner identical with the technique used for growth. It was found that the hydrogen chloride reacts with the silicon appreciably at quite low concentrations. A new removal rate of 50 microns per hour was achieved at 1.25%

hydrogen chloride. At approximately 0.5% trichlorosilane concentration in hydrogen a net growth rate of 50 microns per hour is achieved. It would seem probable that in both the etching reaction and the deposition reaction the net rate is the difference between a forward and a reverse reaction.

It is suggested that the forward reaction might be represented by the following:

$$HSiCl_3 + H_2 \longrightarrow H_2SiCl_2 + HCl$$
$$H_2SiCl_2 + H_2 \longrightarrow H_3SiCl + HCl$$
$$H_3SiCl + H_2 \longrightarrow SiH_4 + HCl$$
$$SiH_4 \longrightarrow Si + 2H_2$$

The reverse reaction might be represented by:

$$2HCl + Si \longrightarrow H_2SiCl_2$$

This equation is suggested because the etch rate with HCl appears to increase with the square of the concentration of HCl. This indicates a second order reaction.

Since experiments on the etching of silicon with hydrogen chloride showed a remarkable degree of polishing, experiments were run starting with lapped silicon.

The silicon had been lapped with 800 lapping compound prior to etching. It was found that mirror-like surfaces can be obtained after removal of between 1 and 2 mils of

silicon by the etching reaction. A series of photos are attached showing the progressive improvement in the finish with increasing amount of silicon removed. See Figures 2.4, 2.5 and 2.6.

2.1.3.1 Epitaxial Structure Delineations;

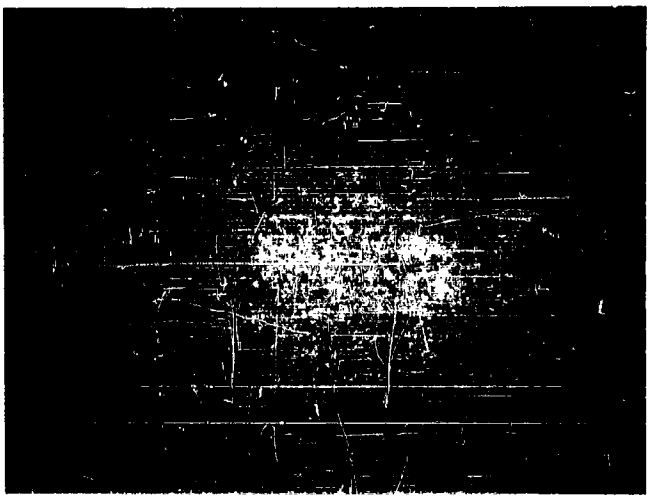
During this period, work was continued on the delineation of epitaxial structures. This effort was expanded to include gallium arsenide as well as germanium and silicon. Both epitaxial and epitaxial-diffused structures were analyzed. Various solid state circuit structures of considerable complexity were studied. Wafers containing as many as six different epitaxial layers were successfully delineated.

2.1.3.2 Oxidations and Phosphorous Diffusions in Silicon

Work was continued in the area of growing silicon dioxide films on exitaxial silicon wafers and then diffusing phosphorous into selective regions of the silicon. Wafers treated in this fashion were then submitted to the appropriate device groups for evaluation as selective circuit functions.

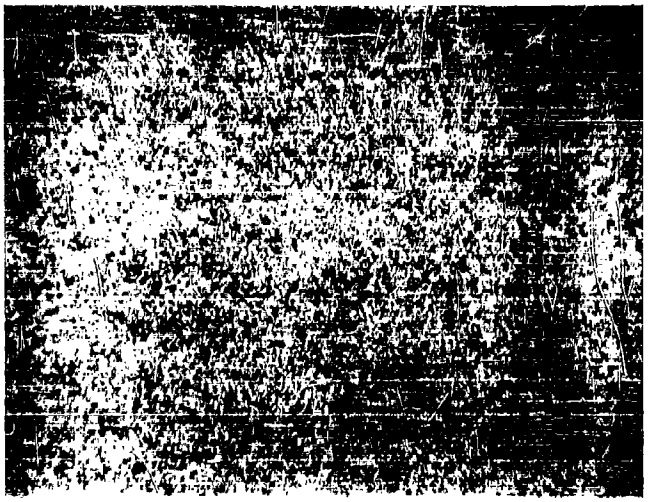
2.1.3.3 Gas Phase Etching

In order to eliminate surface damage caused by the



SURFACE LAPPED WITH 800 MESH LAPPING COMPOUND.

FIGURE 2.4-A

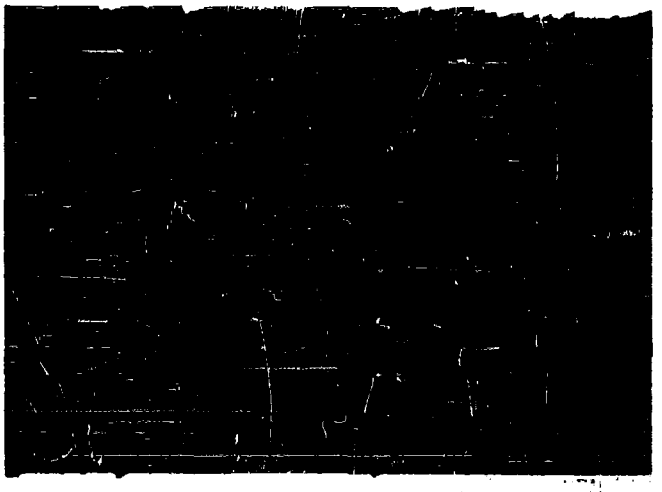


SURFACE VAPOR ETCHED WITH HYDROGEN CHLORIDE AFTER 5 MICRONS REMOVED

FIGURE 2.4-B

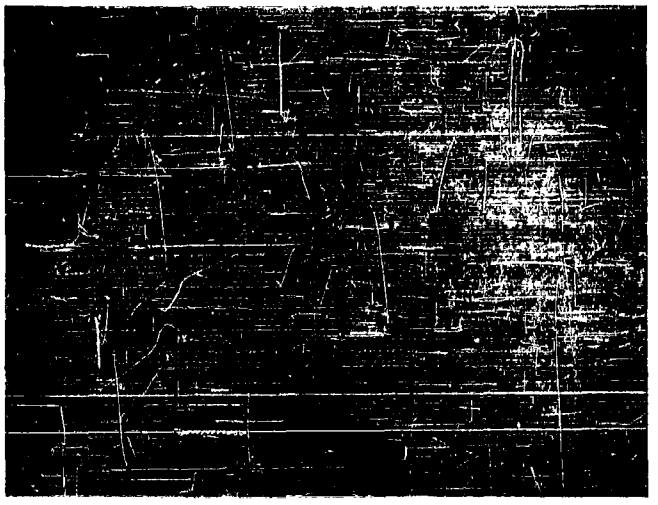
SURFACE AFTER 10 MICRONS REMOVED

FIGURE 2.5-A



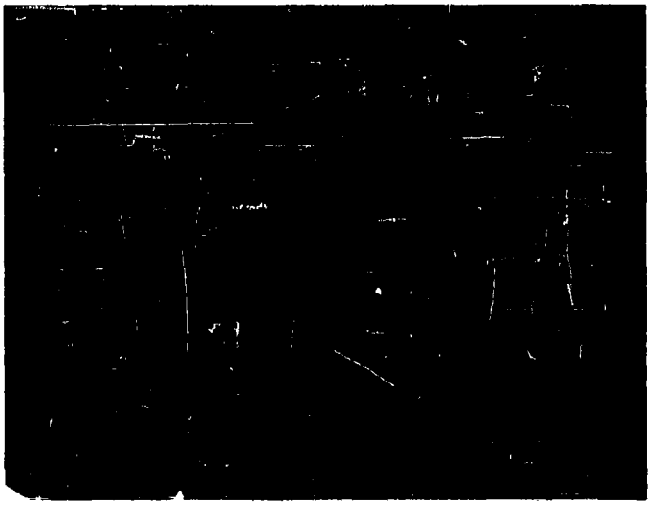
SURFACE AFTER 15 MICRONS REMOVED

FIGURE 2.5-B



SURFACE AFTER 40 MICRONS REMOVED

FIGURE 2.6-A



A SURFACE POLISHED WITH 1/4 MICRON DIAMOND PASTE (FOR COMPARISON)

FIGURE 2.6-B

mechanical polishing of germanium wafers, experiments are being carried out in which several microns of germanium are removed by a gas phase etching method. The etching gas consists of high purity hydrogen chloride. During etching, a chemical reaction occurs as follows:

Ge + xHCl $\longrightarrow$ $GeCl_x$ + $\frac{1}{2}x$ H_2, where x is a positive integer. Hydrogen is generally used as a carrier gas, although some combinations of hydrogen and argon have been utilized. Process variables which are being studied include total gas flow rate, percent composition of hydrogen chloride, and etching time. For lapped surfaces, the surface smoothness of gas-etched wafers approaches, but is not yet completely equivalent to, the quality of mechanically polished surfaces.

2.1.3.4 Heat Treatment of Epitaxial N on N+ Silicon Containing a P-Type Layer

Certain high resistivity N-type silicon films grown on low resistivity arsenic doped substrates have been observed to contain a thin P-type band at the epitaxial-substrate interface. The presence of this layer introduces undesirable Pn Junctions into epitaxial material. To characterize the nature of this P-type band, selective epitaxial samples were heat treated at controlled

temperatures for varying periods of time. The P-type band was observed to widen into the epitaxial film with increasing heat treatment time and then be replaced by an N-type region. This observation is evidence for the theory that the P-type impurity is present as a sheet source at the film-substrate interface. Preliminary data on the rate of widening of the P-type band indicates a diffusion rate for the impurity on the order of that for boron.

2.1.3.5 Masks Against the Diffusion of P-Type Impurities in Gallium Arsenide

An apparatus was constructed, and a procedure developed for depositing approximately 10,000 Å thick layers of silicon dioxide on gallium arsenide. For deposition, gallium arsenide surfaces are exposed to a gas phase consisting of silicon tetrachloride, water vapor, and an inert carrier gas. The material is exposed to this reaction system for a time sufficient to deposit approximately 1,000 Å of silicon dioxide. The material is then annealed at 700°C in argon. By repeating this procedure, thick oxide layers free of cracks can be formed. Such layers are being investigated for their ability to mask against the diffusion of zinc and cadmium.

2.1.4. Masking and Pattern Control of Epitaxial Layers

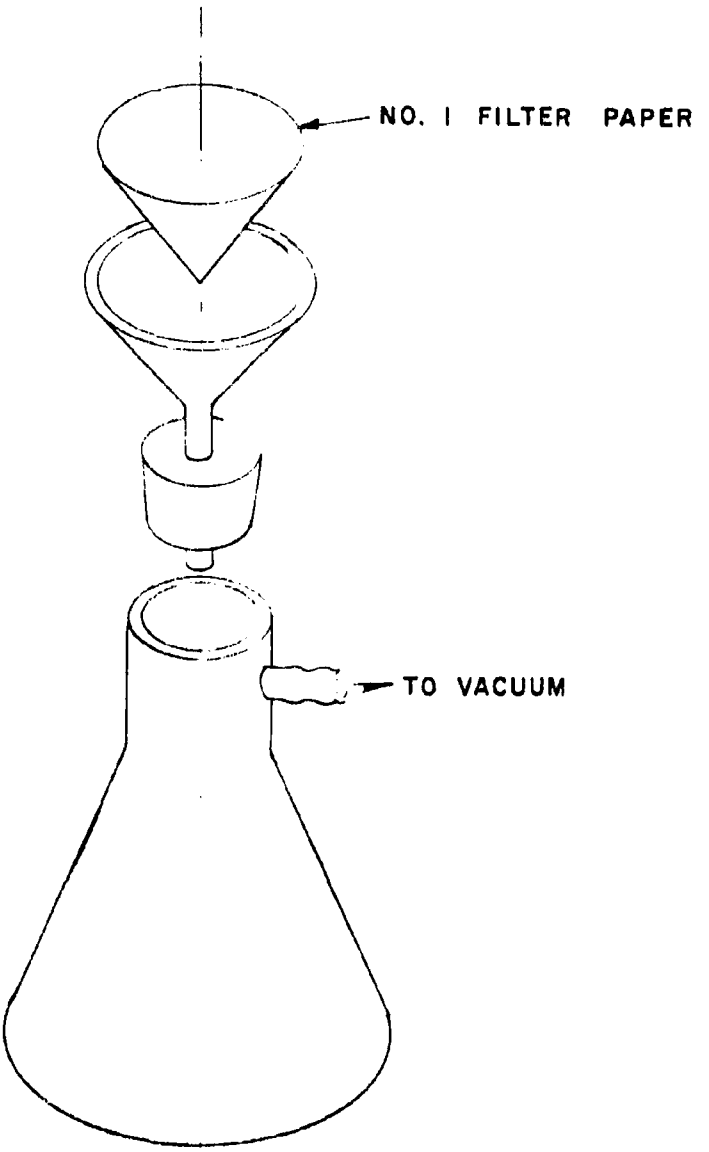
2.1.4.1. Use of KMER as a Mask for Etching Epitaxial Layers

A prerequisite for the fabrication of devices from epitaxially grown layers of different conductivity types is controllable etching of intricate patterns. A number of tests were initiated to determine what was necessary in order to achieve uniform, planar etching when employing "Kodak Metal Etch Resist" (KMER) as a mask. The problems of non-uniform etching was traced to a residue of solid particles left on the surface after normal development and rinse. The residue not only led to a non-planar etched surface, but also prevented accurate studies of time vs. etching rate.

To obtain a residue free surface, two variations in technique were investigated:

1. Filerting of KMER before use.

   Filerting of photoresist materials has been accomplished by a vacuum technique similar to that shown in Figure 2?7. This apparatus, however, was insufficient for KMER since the viscosity of KMER is much higher than that of KPR. Dilution of the KMER in order to use the apparatus was unsuccessful. Consequently, a pressure filter as shown in



VACUUM FILTERING

FIGURE 2.7

Figure 2.8 was constructed. At tank pressures of approximately 50 psi, the filtering rate was 1 ml/minute thus allowing multiple filtering.

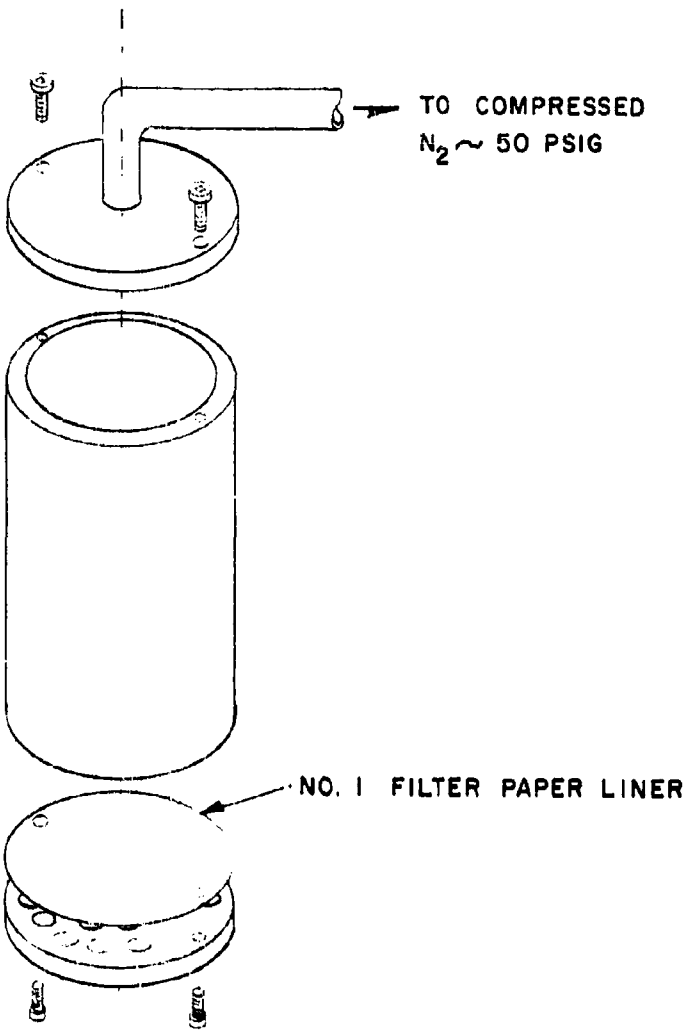
No significant difference was seen between unfiltered KMER and KMER filtered up to four times using this technique.

2. Developing Techniques

Multiple development using fresh solutions had no effect upon the surface film. A spray development using a pasche air brush, however, gave a surface which was apparently free of the film. Etching wafers, which were spray developed, showed that the film was either absent or was reduced to the point where it presented no problem. Comparison of a normally developed sample vs. a spray developed sample is shown in Figure 2.9.

2.1.4.2. Definition Analysis

Optimization of exposure and developing techniques has resulted in well defined patterns enabling the etching of mesas as narrow as 0.0005 of an inch. A structure showing this capability as well as the depth control achieved is shown in Figure 2.10. The structure



PRESSURE FILTERING

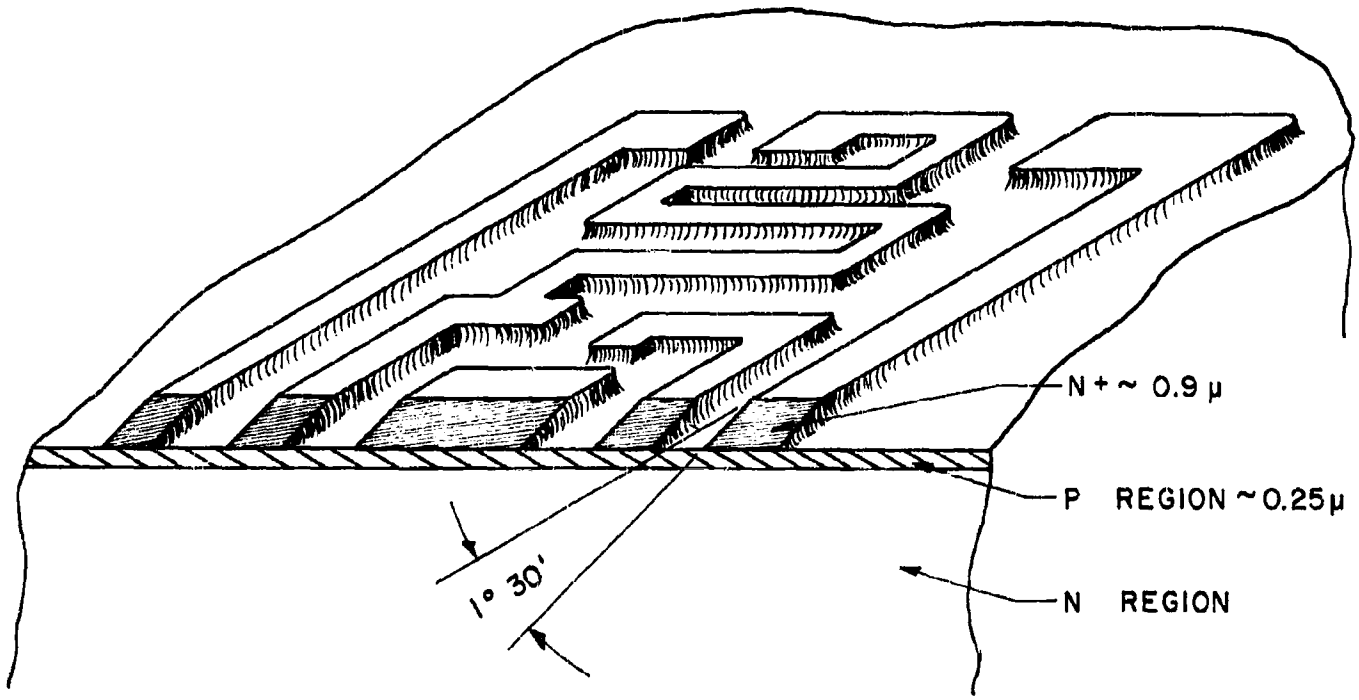
FIGURE 2.8

NORMAL DEVELOPMENT

SPRAY DEVELOPMENT

COMPARISON OF NORMAL vs SPRAY
DEVELOPMENT OF KMER

FIGURE 2.9



BEVELED CIRCUIT CONFIGURATION

FIGURE 2.10

shown here is an all epitaxial configuration. The wafer used for this test was an epitaxially grown $n^+,p,n,n,^+$ configuration with the p region approximately 0.25μ thick. This was too thin to consider metalizing and checking electrically but clearly showed the etching control achieved. [redacted]

2.1.4.3. An Epitaxial NOR Circuit Configuration

Using techniques described in the previous reports a number of of all epitaxial circuits have been fabricated. These units have not had appropriate life time killing techniques applied and are therefore seriously limited in switching times. It is to be noted that the circuit utilized is a 3 resistor input, NOR configuration.

Emphasis during this period has been on fabrication of the NOR function as described in previous reports. The physical layout is as described in the August 1961. report and techniques as described in August 1961 report and in the September 1961 report are employed.

The all epitaxial structure has been chosen as the first priority item for three reasons;

1. The feasibility of constructing an all epitaxial device must be established.

2. The techniques for this process must be developed

3. The material evaluation is a natural by product of this study.

The processing differences in the two approaches are:

1. No high temperature treatment (700°C) of the material after growth is necessary.

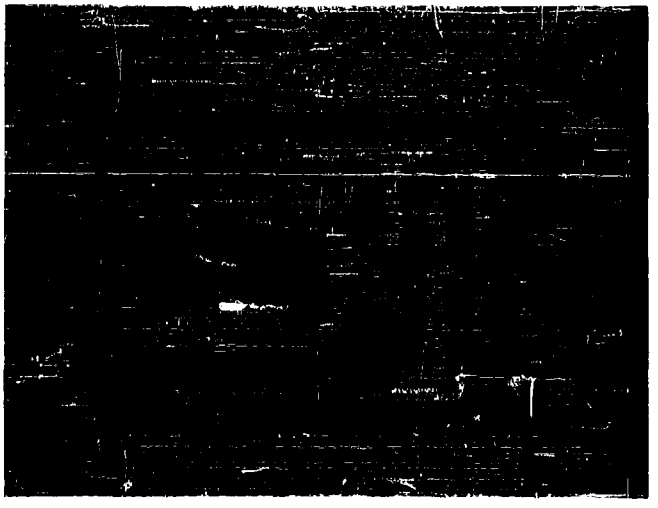
2. The emitter and resistor regions are mesas.

Figure 2.11 shows the KMER pattern for the etch cutting of the emitter and resistor areas on the all epitaxial NOR function. The greatest problem with this step results in areas of sharp corners, such as the collector resistor. The definition is good enough to result in good tolerance (-10%) in resistor values within a given wafer even though tolerances between wafers is larger due to variations in sheet resistivity.

Figure 2.12 shows the definition achieved with KPR for the selective etching of a vapor deposited metallic coating used for contacts. This process is the same whether epitaxial base or all apitaxial structures are used.

Figure 2.13 is a pattern showing the mesa moat etching pattern. It should be noted that the magnification is different on this configuration. This step is the same whether epitaxial base or all epitaxial structure are fabricated.

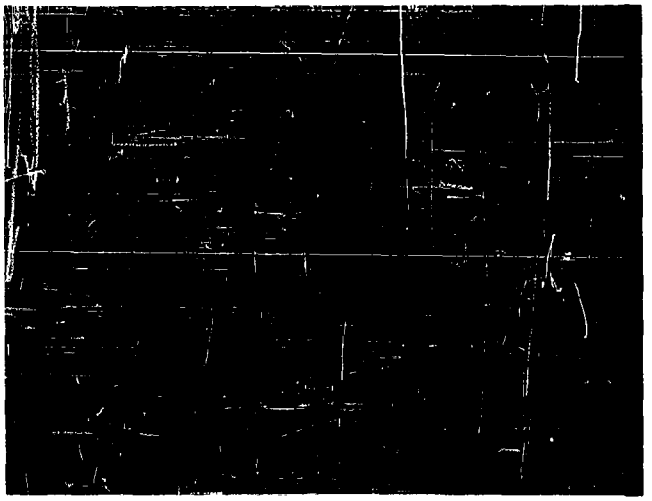
Figure 2.14 shows a microphotograph of a completed unit.



150 X

KMER PATTERN FOR SELECTIVE ETCHING
OF N+ LAYER

FIGURE 2.11



150 X

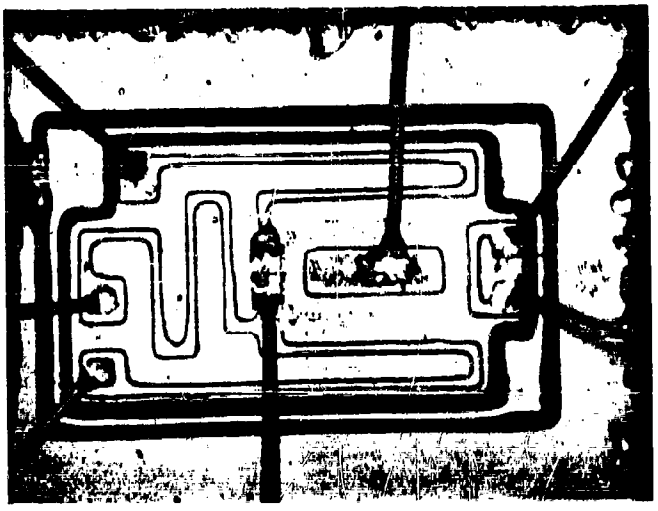
KPR PATTERN FOR SELECTIVE ETCHING
OF VAPOR DEPOSITED METALLIC COATING

FIGURE 2.12

125 X

KMER PATTERN FOR
MOAT ETCHING OF UNIT

FIGURE 2.13



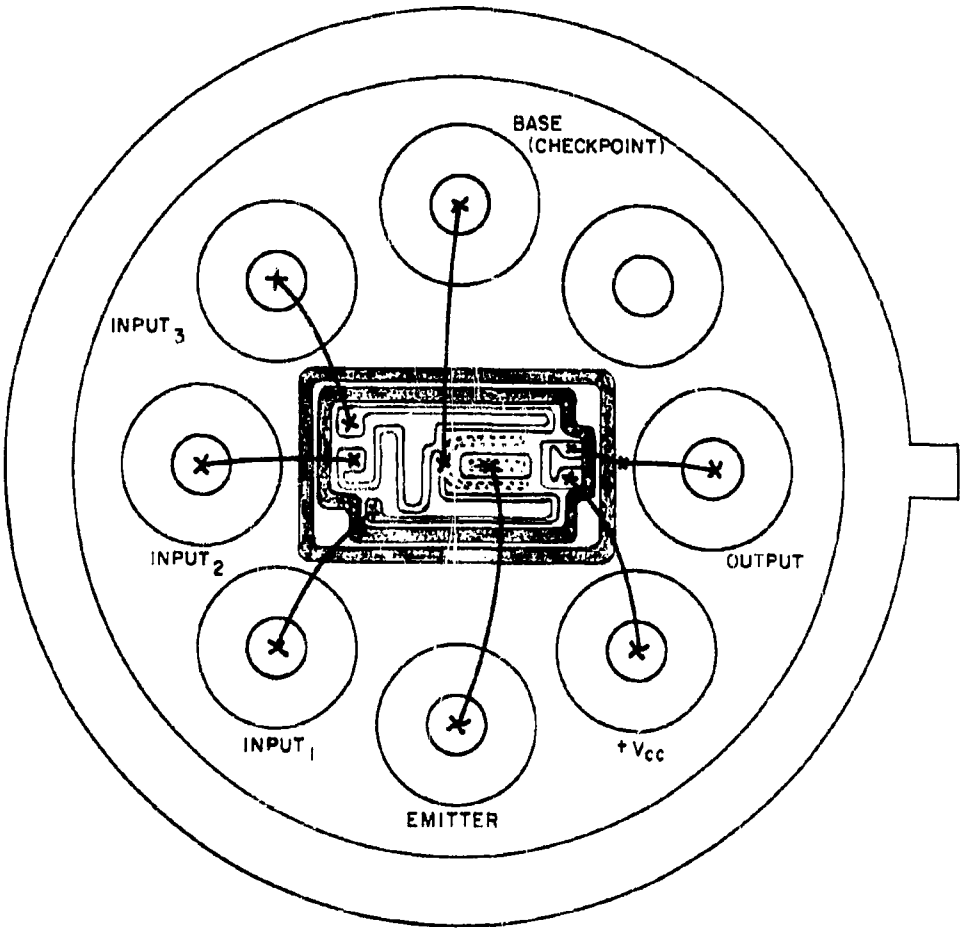
NOR CIRCUIT MOUNTED ON HEADER

FIGURE 2.14

The unit shown is mounted on an 8 lead TO-5 header with connections as shown in Figure 2.15.

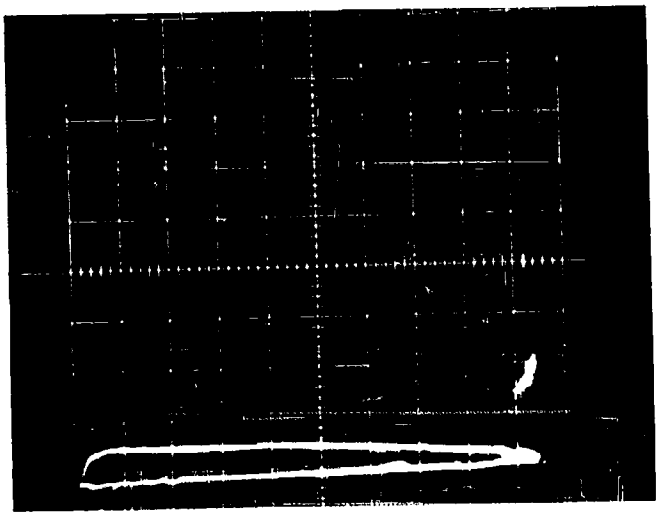
Figures 2.16,2.17, 2.18 and 2.19 show the transistor characteristics of the NOR circuit. These characteristics are of a unit before the output lead is connected. After connection of this lead the "collector to base" voltage and "collector to emitter" voltage are determined by the voltage breakdown of the "emitter to base" junction thru the back biased collector resistor. Since this circuit was designed for +6 volts operation this is of no consequence. If operation above 10 volts is desired a modification in resistor configuration is necessary. Figure 2.16 is the "collector to base" breakdown at 10us/division vertically and 10V/division horizontally. Figure 2.17 is the "collector to emitter" breakdown with I_b=0, V_{CE}=10V/division horizontally and I_C =10ua/division Vertically. Figure 2.18 "emitter to base" breakdown characteristic scales are: 10ua/division vertically and IV/division horizontally. Figure 2.19 is the common emitter current gain of this device scales are 1ma/division vertically, 1 Volt/div. horizontally and base input steps of 0.1ma/step.

Figures 2.20 and 2.21 show the linearity of the resistors obtained. Figure 2.20 shows the base input resistors of the device which are linear to 9.5 volts and have a resistance



HEADER CONNECTIONS FOR ALL EPITAXIAL NOR CIRCUITS

FIGURE 2.15

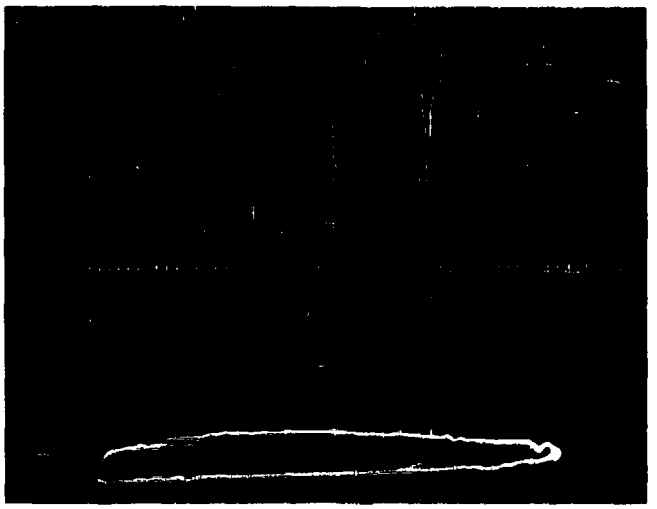


COLLECTOR TO BASE BREAKDOWN CHARACTERISTIC

I_C = 10 μa/DIV VERT.

V = 10 V/DIV HORIZ.

FIGURE 2.16



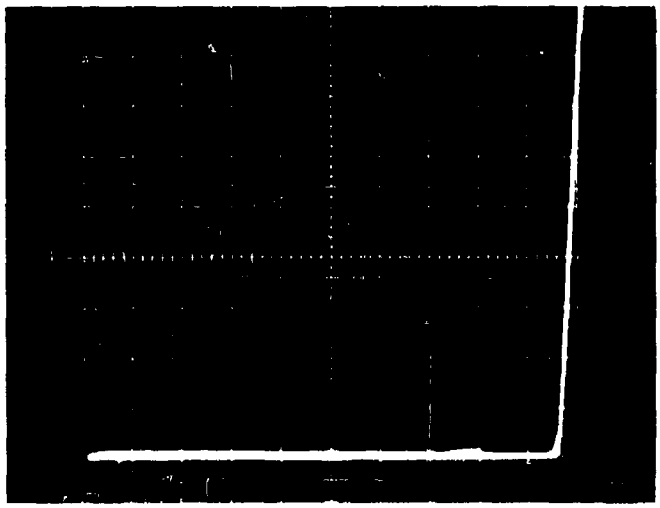
COLLECTOR TO EMITTER BREAKDOWN CHARACTERISTIC

I_C = 10 μa / DIV VERT.

V_{ce} = 10 V / DIV HORIZ.

I_B = 0

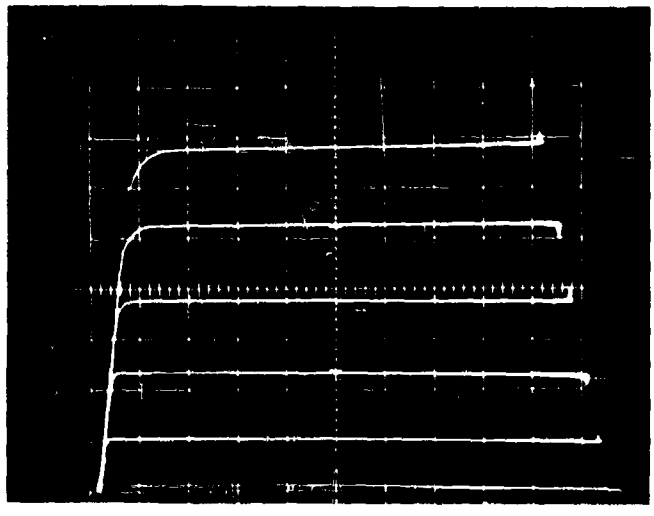
FIGURE 2.17



EMITTER TO BASE BREAKDOWN
CHARACTERISTICS

I_c = 10 μa/DIV VERT.
V_{eb} = 1 V/DIV HORIZ.

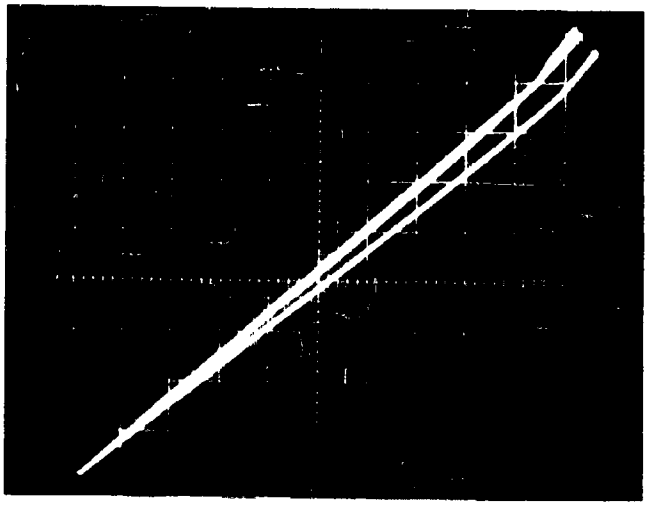
FIGURE 2.18



COMMON EMITTER CURRENT GAIN
(h_{fe})

I_C = 1 ma/DIV VERT.
V_{ce} = 1 V/DIV HORIZ.
I_B = 0.1 ma/STEP

FIGURE 2.19



BASE INPUT RESISTORS

I = 0.2 ma/DIV VERT.
V = 1.0 V/DIV HORIZ.

FIGURE 2.20

of 6000 ohms (with one at 6500 ohms. Figure 2.21 is a collector resistor which has a resistance of 750 ohms which again is linear.

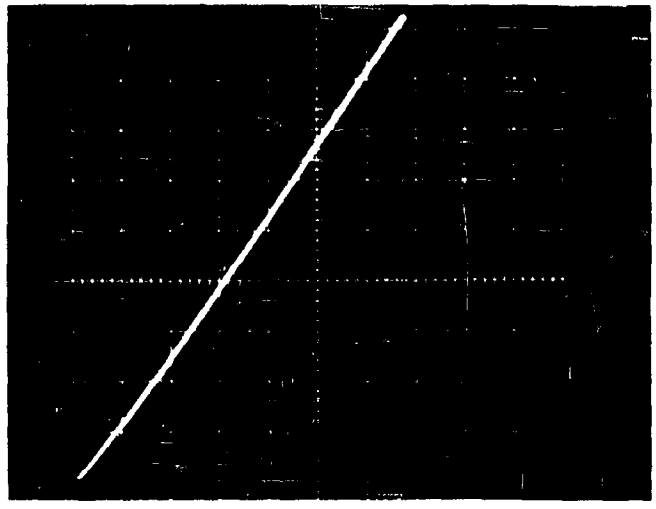
It is anticipated that work on a versatile amplifier circuit, as shown schematically in Figure 2.22 will be initiated soon. This will follow along the same lines as the monolithic NOR circuit. This particular circuit should be useful from D.C. to possibly 70 mc, depending on the external element placed between points 1 and 6.

It is anticipated that much can be gained by use of low temperature glass as a passivation technique coupled with the monolithic epitaxial approach. The low temperature passivation technique developed by the new process group of Motorola Semiconductor Division has been applied with considerable success.

3.0 Thin Film Technology

3.1 Deposition of Glass Films

This task goal is to develop means for depositing glass films on semiconductor substrates which are compatible with other thin film and semiconductor materials and technologies. Low temperature reactions are being investigated for depositing silicon dioxide films which are non-crystalline onto cold or relatively cool substrates.

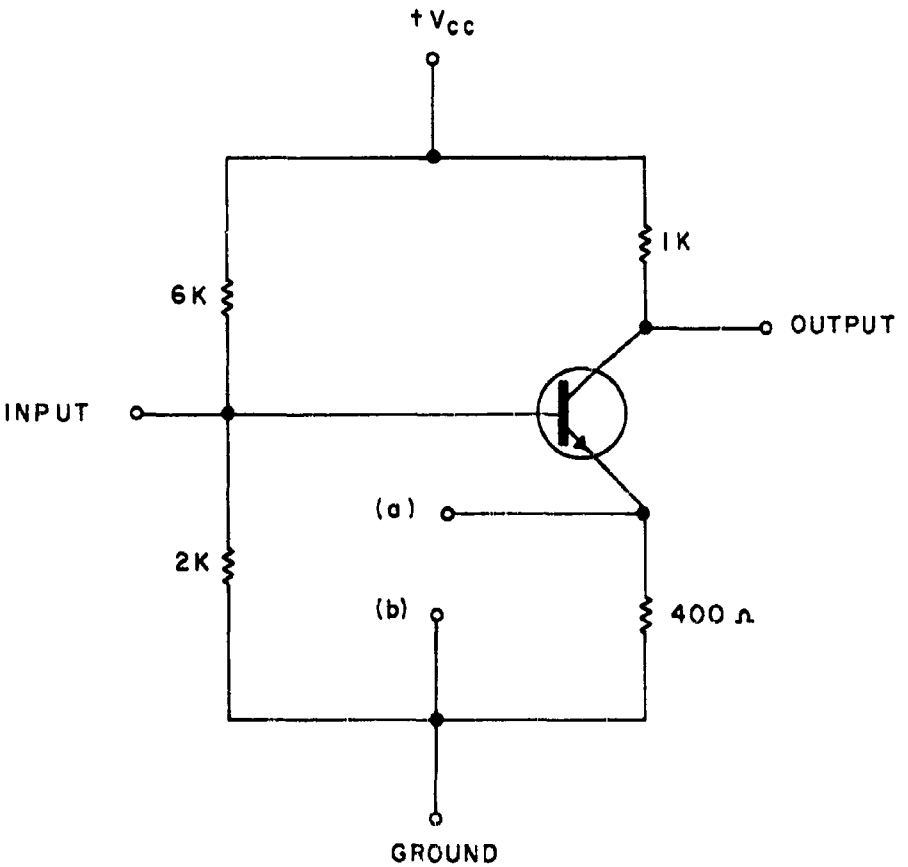


COLLECTOR RESISTOR

I = 1 ma/DIV VERT.

V = 1.0 V/DIV HORIZ.

FIGURE 2.21



VERSATILE AMPLIFIER FOR CONSIDERATION

FIGURE 2.22

These glass films are being investigated for use as (a) dielectric film for capacitors, (b) an electrical insulating film for conductor cross-over insulation, (c) an encapsulant film for thin-film components.

During this period some results were obtained on use of a mixed titania silica glass as a dielectric for capacitors. This mixture was pursued in that titania is known to have a dielectric constant in the order of 100 and thus should provide a large amount of capacitance per unit area of a single dielectric layer capacitor. The pure titania films proved to be poor electrical insulators, undoubtedly due to the nonstoichiometric ratio of titanium and oxygen. In an attempt to improve the leakage resistance of capacitors made with this dielectric, silica was introduced into the glass system. Preliminary results of capacitors constructed with titania (25%) silica (75%) dielectric are given in Table I. The dissipation factor and capacitance was measured at 10 megacycles while the leakage current was measured at 10 volts. The capacitors were deposited on quartz substrates at 100°C and had aluminum bottom electrodes and silver counter electrodes. X-ray examination of films produced in a similar manner indicated the absence of a crystalline phase. With titania films 3000 Angstrom units thick deposited on quartz substrates

TABLE 1

Cap No.	C uuf	D.F. %.	I_L amperes
1	50	2.7	2.5×10^{-8}
2	75	5.0	7×10^{-6}
3	56	3.0	7×10^{-6}
4	51	3.0	2.5×10^{-7}
5	104	6.6	3×10^{-8}
6	120	6.3	5×10^{-8}
7	150	5.0	5×10^{-8}
8	150	6.0	5×10^{-8}
9	95	3.6	5×10^{-8}

by gas plating techniques, the dielectric constant is about 35. Capacitors formed with aluminum electrodes failed between 50 and 100 hours. Under environmental tests at 200°C the titania underwent reduction through interaction with the aluminum electrode. The aluminum electrode metal becaue transparent and a bluish-brown color of the partially reduced titania was observed. Other electrode materials were evaluated including gold, copper and tin, but none were found satisfactory with respect to yield or leakage current.

3.1.1 Silicon Monoxide Dielectrics

A program was initiated during this period to study the application of silicon monoxide dielectrics to semiconductor substrates. The means for deposition is vacuum evaporation, a fairly standard technique in the industry. Although vacuum processes have disadvantages in that vacuum equipments are required and that the thc processing could be expensive as compared to vapor-deposited films, the vacuum deposition has these advantages:

1. The thickness of the dielectric films can be more readily reproduced than those applied by gas plating techniques.
2. The vacuum deposition process enables the use of

shadow type masks to delineate those areas on the substrate to be covered by the dielectric material.

The present program was initiated to determine the aging characteristics of such films at high temperatures and under voltage stress and also to determine the use of this material as a dielectric at high frequencies. During this period, twenty-four capacitors were constructed utilizing silver electrodes and dielectric thicknesses varying between 60 and 120 Angstrom units per second. The silicon monoxide was evaporated from a cylindrical alumina crucible with imbedded molybdenum filament. The substrates were initially heated to 350°C and then cooled to 200°C in vacuum prior to receiving the silicon monoxide deposition. The substrates were allowed to cool before venting the bell jar. The results can be summarized briefly as follows:

1. All capacitors were initially functional and none of the films crazed or peeled.
2. After thermal cycling between -18°C and +125°C and a thermal aging period of 24 hours at 125°C during which they were subjected to 10 volts dc electrical stress, all units were functional. During subsequent leakage measurements at 10 volts dc, five units shorted. This is believed to be due to the measurement technique and the handling process.

3. The dielectric constant calculated to be between 10.1 and 10.8. The average dissipation factor after aging was 1.37% at 50 megacycles.

In order to control the dielectric constant, one must control the degree of disassociation of the silicon monoxide during the evaporation or the degree of combination of the silicon monoxide with residual oxygen within the vacuum chamber. By controlling the oxygen partial pressure and evaporation rate, it is believed possible that reproducible dielectric constants will be obtained. A rapid evaporation rate at high vacuum will tend to deposit a film which is rich in silicon. A slow evaporation rate at high oxygen partial pressure will tend to produce a quartz or S_iO_2 rich film. The dielectric constant of S_iO_2 is roughly four while that of silicon is eleven. Thus it is believed possible to deposit this material having delectric constants varying between four and eleven. To aid in the control of the dielectric constant the construction of an evaporation rate monitor was undertaken.

The rate monitor was based upon the exchange of momentum between a portion of the vapor and a sensitive torsion gage. The torsion gage consists of a sensitive micrometer movement which has been modified by adding an arm and a vane to the movement. A portion of the silicon monoxide vapor

is caused to impinge upon this vane producing torque on the sensitive movement. A controlled electrical current is then caused to flow through the movement to counter the torque due to the momentum of the silicon monoxide vapor. A measurement of this restoring current indicates the momentum of the vapor. The sensor then is a function of the total mass of the material evaporated as well as the velocity of the vapor. The sensor, therefore, is sensitive not only to the rate of deposition but is also a function of the source temperature. Utilizing constant or relatively constant source sizes, a given rate of evaporation will occur at a fixed temperature. Thus the momentum sensor can be calibrated as a rate monitor.

The rate meter was designed in order to control the dielectric constant of the resultant silicon monoxide film as well as to control the thickness of the deposited film. In use, oxygen is bled into the vacuum chamber until a pressure of 10^{-4} mm of mercury is achieved. At that time, the evaporation rate is increased until 60 Angstrom units per second is observed. A shutter is then opened to allow this stream to deposit upon the substrate and is timed to be open for a pre-determined number of seconds to control the thickness of the deposited film. To aid in maintaining a constant rate of evaporation, an isothermal chamber

was constructed as the evaporation crucible. The rate monitor indicates that having once established a given rate of evaporation, this evaporation rate remains constant for a period greater than 10 minutes.

Utilizing the completed equipment, tests were made to determine our ability to deposit capacitors of desired values. A series of two runs were made to form capacitors with values of 95 mmfd. The first run produced units ranging from 86 to 98 mmfd with a mean value of 98 mmfd, while the second run resulted in capacitor values ranging from 83 to 93 mmfd with a mean at 90 mmfd.

Emphasis was then placed upon the lowering of the dissipation factor of silicon monoxide capacitors at high frequencies. Capacitors constructed with silver electrodes exhibited extremely low breakdown potential (less than 15 volts) and a 70% failure rate at 250 hours aging at 125°C with 10 volts of stress. Aluminum electrodes provided capacitors with consistant aging characteristics, high breakdown potentials and low leakage currents, with a disadvantage that the dissipation factors were somewhat higher than those exhibited by the silver electroded capacitors. Capacitors of three to four mmfd values, constructed with aluminum electrodes, exhibited leakage currents in the order of

10^{-13} amperes when 10 volts were applied to them and possessed dissipation factors in the order of 2% at 100 megacycles. The breakdown potentials of these capacitors was determined to be approximately 590 volts.

An attempt to use silver electrodes with aluminum barrier overlay films next to the dielectric was not successful. During substrate heating the aluminum and silver diffused into one another forming a surface to which the silicon monoxide does not readily adhere. Gold electrodes produced shorted capacitors.

3.1.2. SiO_2 Films

A group of sixteen SiO_2 capacitors were constructed during this period and placed under environmental tests. The glass film was deposited onto quartz substrates. Sixteen capacitors, with values ranging from 50 uuf to 600 uuf were formed. The glass films showed slight thickness gradients and were in the order of 1000 Angstrom units thick. The initial dissipation factors measured at 1000 cycles ranged between 2 to 5 percent and the leakage current was less than 10^{-9} amperes at 10%. The dielectric values were calculated to range between 5 and 10. It is suspected that these films contain a considerable amount of water. Certainly they contain a hydrated interface

between the outer electrode and the dielectric. Such an interface could introduce dipoles to enhance the apparent dielectric constant of the glass and also contribute to the dissipation factor.

All of these capacitors were placed on environmental tests at 200°C, but SiO_2 films made by identical techniques were employed for further evaluations.

A film thickness of 3000 Angstrom units was formed in a period of 10 minutes. Aluminum electrodes were utilized to evaluate the dielectric properties of the films. Figure 3.1 represents results in change of capacitance and average dissipation factor for an initial group of 19 capacitors placed under environmental test. Between 25 hours and 75 hours at 200°C five of the 19 capacitors were lost due to shorts. In the period between 75 and 100 hours, two more capacitors were lost due to shorts. The capacitance value and the dissipation factors decreased during the first 100 hours of environmental stress at 200°C. These effects can be attributed to the removal of water molecules which may actually be chemically bonded with as well as absorbed on the silica network. The best estimate to date of the dielectric constant of the silica, as deposited, is between 5 and 6. (The major source of measurement

error is introduced in determining thickness.) The excess dielectric constant over the value of four for pure quartz is attributed to the presence of water molecules.

In the life test evaluation of these capacitors in the period between 100 hours and 150 hours, the oven temperature regulating mechanism malfunctioned. The temperature as noted at the end of 150 hours was 250°C. No additional capacitors were lost of the remaining 12 during this period of increased environmental stress and no capacitors were lost after the temperature was reduced to 125°C and subjected at that temperature for an additional period of 550 hours. The apparent increase in capacitance as well as dissipation factor during the period of high temperature bake of 250°C for 50 hours is not yet explained. After the a50°C stress period, both the capacitance values and the dissipation factors observed did not change appreciable in value. The dissipation factor measured at 1 kc was 1.5%.

Infrared transmission spectra of these films deposited on rock salt substrates corresponded to those observed with SiO_2 films deposited by vacuum evaporation techniques. The X-ray diffraction spectra do not suggest any crystalline nature of these films. A capacitance value of 0.2 mmfd per square centimeter appears to be optimum for these films.

DC leakage currents observed for 60 mmfd capacitors is in the order of 10^{-10} amperes when 10 volts is impressed across them. This indicates a resistance value of 10^{11} ohms. Breakdown voltage is near 100 volts.

3.2 Tantalum Oxide Capacitors

Compatible techniques are being sought for constructing tantalum thin-film capacitors onto semiconducting substrates. The tantalum oxide capacitor is attractive in that a large capacitance can be achieved in a small area with this component.

Initially, a total of 88 capacitors were produced utilizing a layer of chromium and then gold as the counter electrode. The capacitors were anodized at 50 volts in 5% ammonium orthophosphate electrolyte. The yield of this particular run of capacitors was 90%. These results indicate that the problems of shrinkage which were experienced earlier have been essentially brought under control.

Low dissipation type capacitors constructed earlier, utilizing an aluminum film underlay prior to the deposition of tantalum films, had been placed on environmental life tests at 115°C with 10 volts applied. These capacitors were constructed utilizing chrome gold electrodes. All

capacitors failed under this environmental condition within 40 hours. Capacitors were then prepared to determine the cause of failure. Fifty-two capacitors were constructed utilizing various electroding schemes to determine what material induced the failure. These were: (a) capacitors constructed of tantalum, tantalum oxide and aluminum, (b) capacitors constructed of aluminum, tantalum, tantalum oxide, gold, (c) capacitors constructed with tantalum, tantalum oxide, chromium and gold, and (d) capacitors constructed with aluminum, tantalum, tantalum oxide, chromium and gold. The capacitors were designed to have a breakdown voltage of 50 volts and a capacitance of 1100 uuf. Those capacitors considered acceptable were determined to have leakage currents less than 10^{-9} ampers when 10 volts were applied to the capacitor with the tantalum film positive. The per cent yield of capacitors experiences is as follows:

Type A	100%
Type B	83%
Type C	64%
Type D	29%

The overall percentage yield was 67%. Experience from this run of capacitors indicates that they can be constructed to within a tolerance of 6.8% rms from the mean.

Under environmental tests the source of failure was positively attributed to the thin chromium film used between the tantalum and the gold counter electrode to provide a highly adherent electrode. The test capacitors were constructed to have nominal values of 1500 uuf and a breakdown voltage of 50 volts. When placed under a thermal stress of 125°C and a voltage of 20 volts, all of the chromium layer capacitors shorted within a period of 66 hours. The remaining chromed capacitor exhibited a large leakage current. In general, other capacitors constructed without the chrome are behaving quite normally and are still under environmental tests. The elimination of the chromium film is expected to privide highly stable capacitors even when aluminum backing is utilized to reduce the dissipation factor. Previous experience has indicated that tantalum capacitors constructed without the chromium or aluminum have exhibited excellent lifetime characteristics when placed under thermal and electric stress for periods of 1500 hours.

A total of 66 capacitors were constructed utilizing aluminum, tantalum, tantalum oxide and gold. During vacuum deposition of the tantalum electrode, preheating of the substrate is employed. In the past, a simple nichrome heater was used; however, recently a prefocused

100 watt projection lamp has been employed for preheating. During the construction period for building these capacitors, the heating bulb became defective and was not observed to be defective until about two-thirds of the run was completed. When using the defective heating bulb, a yield of 60 percent was achieved. When the defective bulb was replaced, a yield of 92 percent was obtained. All of the capacitors had aluminum underlying the tantalum and were anodized at 100 volts in 5 percent ammonium orthophosphate electrolyte. Leakage current for the acceptable capacitors was arbitrarily taken to be less than 10^{-9} amperes when 10 volts were applied.

Effort was then devoted to the study of means for reducing the dissipation factor of tantalum capacitors at elevated frequencies. These capacitors provide rated voltage-capacitance products of 5 mfd-volts per square centimeter. It was attempted to construct capacitors within an area of 1 millimeter by 1 millimeter with values of 1000 mmfds and breakdown voltages in excess of 25 volts. It is further desired to have a series resistance of equal to or less than 1 ohm and a parallel resistance of greater than 1 megohm. At the end of this report period, of the total of 84 capacitors placed under construction

for this evaluation, 24 have been completed and leakage and electrical tests made on them. Of the 24 capacitors tested at 10 volts, 18 possessed leakage currents less than 10^{-9} amperes when 10 volts were impressed across them, providing a yield of 75%. The test capacitors were formed at 50 volts rather than the desired 100 volts thus the capacitance values were nearly double that of the desired 1000 mmfd. The breakdown potentials of these capacitors are very close to 50 volts in the forward direction. When operated at 25 volts over a long period of time, their stability has proven to be excellent. Parallel resistance of these capacitors was in the order of 10^{10} ohms, and the dissipation factor at 100 kc appears to be in the order of 1%. This indicates series resistance of approximately 10 ohms.

Current studies are being made as to the cause of the high dissipation factor. Plots made of the dissipation factor vs. frequency indicate that the lowest dissipation factor over the frequency range from a few tens of cycles to the megacycle region was in the order of 1/2 of 1%. Recent studies indicate that most of this resistance is attributed to the junction between a conductor film and the tantalum electrode. Apparently the tantalum forms an oxide

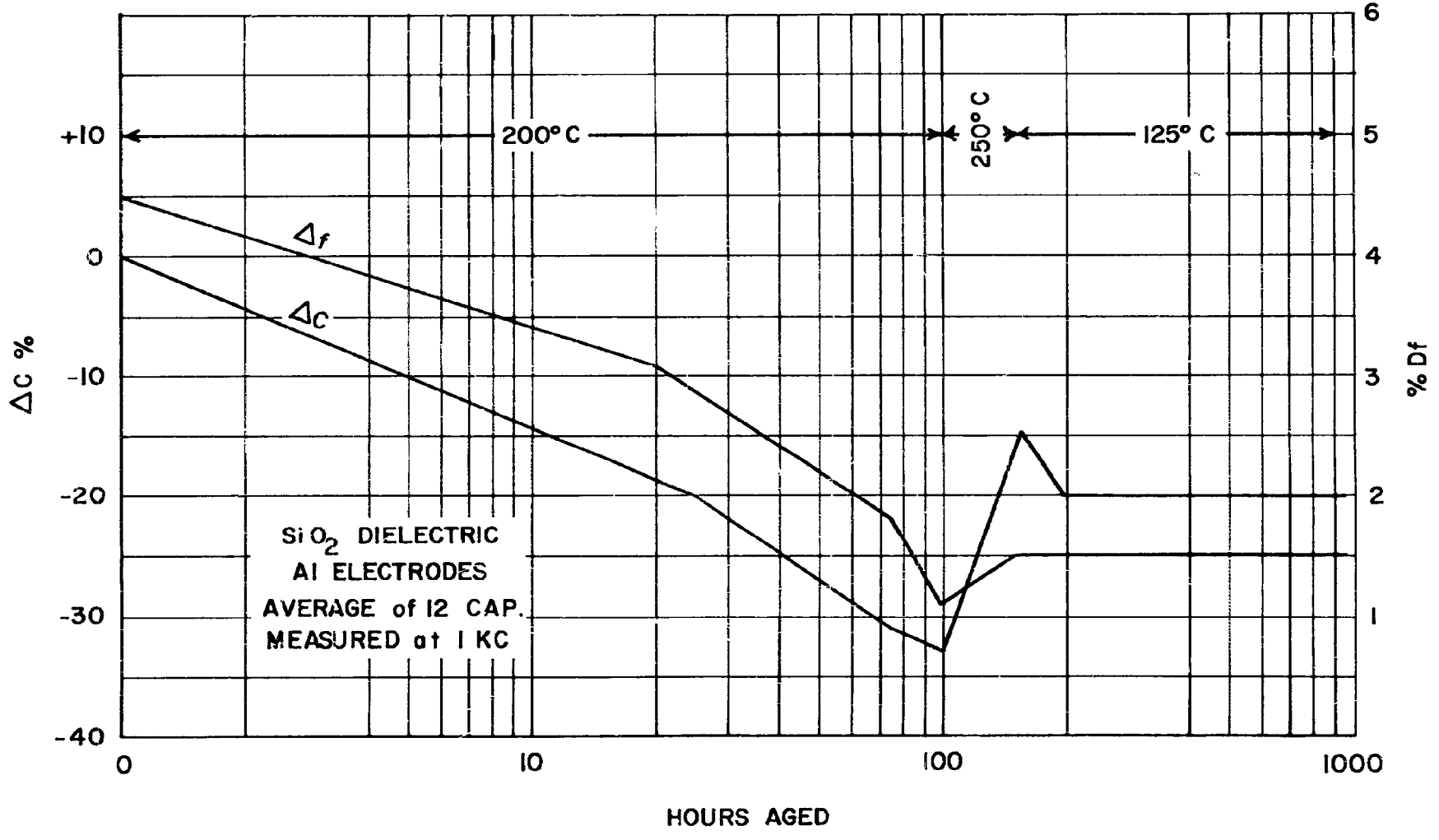

+10
0
-10
-20
-30
-40
ΔC %
200° C
250° C
125° C
Δf
ΔC
SiO2 DIELECTRIC
Al ELECTRODES
AVERAGE of 12 CAP.
MEASURED at 1 KC
0
10
100
1000
HOURS AGED
6
5
4
3
2
1
% Df

FIGURE 3. 1

layer at this interface, preventing the desired low ohmic contact. The dissipation factor minimum, observed when an attempt was made to decrease this resistance, was 0.13%. It appears, therefore, that it may be possible to approach the desired series resistance of 1 ohm with such a capacitor. Efforts will be devoted during the next period to demonstrate this capacility utilizing silicon crystals as substrate materials.

In a program to devise a rapid electroding technique which does not require a large tantalum area for making electrical contact during the anodizing process, a method has been devised which requires only a spot 1mm in diameter. The use of tiny tantalum wires will be explored during the coming report period.

3.3 TIN OXIDE RESISTORS

The use of semiconducting materials as thin film resistors is of interest to this program in that they provide a large value of resistance in a small substrate area. This particular program has been initiated to determine means for depositing thin films of tin oxide on semiconducting substrates at low temperature. The general technique is to utilize gas plating. The methods studied employed tin halide to form the tin oxide films. In this process, the reaction takes place at atmospheric pressure. The results indicate that a minimum substrate temperature of 250°C is required in order to produce hard films of tin oxide.

Conductive films were produced at substrate temperatures of 300° C. In general, all films deposited at temperatures below 300 °C could be made more conductive by subsequent heating at 500 °C in air.

Means were explored for doping tin oxide films. Phosphorus trichloride, when added to the tin halide vapor, produced films which were thick, yellow in color, and non-conductive. The use of isopropl antimonide as a dopant, was unsuccessful in that undesirable organic residue was introduced into the film.

Equipment was set up for measuring Hall voltages and for taking X-ray analysis of the tin oxide films. Films deposited at substrate temperatures of 300 °C showed N-type semiconducting character. X-ray analysis of these films indicated a high degree of amorphism in the films. Films deposited at 550 °C substrate temperature indicate a highly ordered crystalline structure containing a large number of tiny crystalites.

Continuous films of tin oxide have been deposited on substrates maintained at low temperatures. The films ranged in thickness from 1000 to 3000 Angstrom units and exhibited extremely high resistivities indicating near stoichimetric tin oxide. The films were formed by gas plating techniques. Subsequent work along this line will study the feasibility of adding group three or group five elements as P or N type dopants to modify the conductivity.

3.4 NICHROME RESISTORS

During this period, the various parameters required to deposit stable nichrome resistors were studied. Parameters such as evaporation rates, substrate temperature, and annealing procedures are being explored in order to determine the best method for depositing stable resistors

The first evaluation sample was of nichrome resistors made with 250 ohms per square material. Unencapsulated films made with this material were aged at 125°C for 600 hours, and have indicated typical increases in resistance of 5.5%. This aging has been continued and the results will be evaluated at a later date. Films of 225 ohms per square deposited on ceramic substrates exhibit a 4% increase in resistance during a vacuum anneal period at 350°C for one-half hour. Those films which were not annealed but were immediately placed in life-time tests at 125°C in air have shown increases in resistance of between 7% and 10% for a period of 1194 hours. Several Nichrome resistors have been constructed, aged, and placed under a life test with and without silicon dioxide encapsulation.

The temperature coefficients or resistance in the range between 0 and 100°C appear to be less than 100 parts per million per degree centigrade. Besides the aging test currently underway, studies will be made as to the compisition of a

deposited film versus source temperature. Correlations will be made with this and the various aging characteristics and temperature coefficients observed.

Considerable additional effort has been spent in arranging the vacuum deposition apparatus so that an electron bombardment technique could be utilized for evaporating nichrome metal. This is desirable to prevent contamination of the vapor through alloying and reacting with the hot crucible. Aging data of nichrome resistors encapsulated with silicon dioxide glass showed a total percent increase in resistance of less than 1% over test periods exceeding 800 hours at 125° C. The average for seven samples was 0.7% increase in resistance for this time period. Another group of nichrome resistors deposited at 250 ohms per square, encapsulated in glass, and subjected to 125°C for 200 hours, increased in resistance an average of 0.1%. The results of this data indicate that the major cause for nichrome resistance agins is not reorientation of the crystalline structure of the film, but is due to oxidation of the resistor surface. The tests also indicate the excellence of the glass encapsulant process. The films reported on the above consisted of a nickel chromium iron film, 62% nickel, 21% chromium and 15% iron. The evaluations of

80% nickel, 20% chromium films were also made during this period. In general, the resistivity of this material is less than that of nichrome containing 15% iron. The resistivity appears to be 2.5×10^{-4} ohms centimeters with 80% nickel, 20% chromium films as opposed to 3.5×10^{-4} ohms centimeters for nickel chromium iron films. Initial experience indicates that the 80% nickel, 20% chromium films stabilize more quickly than do those containing iron.

4.0 CIRCUIT CONSIDERATIONS

In order to evaluate device and process techniques, a study has been started to pick "circuit examples" in a wide range of applications. Four areas of study are suggested:

1. RF and IF circuits, including VHF receivers and transmitters.
2. Servo and audio amplifiers - including DC
3. Power supply circuits
4. Digital logic circuits

The problem areas in VHF circuits appear to be selectivity, stability, and gain at the very high frequencies. A unique circuit approach including tuned elements in the emitter lead appears to offer a solution to these problems.

Except for high power levels and complexity, the servo and audio amplifier circuits seem rather easily adaptable to integrated circuits.

Motorola has been a leader in the production of zener diodes which are a natural for the voltage regulated power supply function. A "chopper" type regulator which can reduce dissipation considerably will be considered for integrated circuit work.

The digital logic blocks currently available for integrated circuit computers are too slow for modern designs. A series of high speed logic blocks is proposed.

Additional work is planned to study the performance of R, L, C components on semiconductor substrates of varying resistivities. The problem is the presence of low resistivity material in capacitive and inductive fields. This effect substantially reduces available circuit Q.

4.1 Band-Pass Amplifier

L C, band-pass amplifiers, at frequencies below 5 MC require values of inductances which are presently beyond

the Integrated Circuit capability. In an attempt to eliminate the need for large value inductors, a number of devices are currently being investigated. Listed below are a few examples of devices which will provide a band-pass characteristics, sans inductance.

1. Ceramic and Crystal Filters
2. R. C. Network Active Filters
3. Semiconductor phenomenon (Minority Carrier Delays)
4. Magnetostrictive Filters

The investigation of the above devices are carried out on a broad basis. In each, the study provides information on such items as compatibility with existing integrated circuit technologies as well as listing the limitations and advantages of the approach.

As a final phase of the study program, a circuit is designed, breadboarded, and evaluated in order to determine the validity of information gained in the study phase.

To date, work on Item 1, Ceramic and Crystal Filters, and Item 2, R. C. Network Active Filters, has been completed. The final report which discusses advantages, limitations, design procedures, as well as other incidental information, has been prepared.

4.2 Low-Pass Amplifier

The combination of low frequencies and the transistor, a low impedance device, requires that large value capacitors be used as by-pass and interstage coupling components in most amplifier configurations. The goal of the study program in the low-pass amplifier area is to find methods which will reduce in value or eliminate completely the large value capacitors.

There are two approaches to the problem currently under investigation. The first eliminates the need for capacitors by specifying that the device be direct-coupled. This is perhaps an oversimplification for in many instances the elimination of capacitance from coupling networks creats new problems which are difficult to overcome. The study program for this area has been completed and a report entitled "General Purpose Voltage Amplifier Design Study" has been published.

In many cases it is not necessary to provide a band-pass function which will include D.C. For instance, general purpose speech amplifiers require a low frequency cut-off of approximately 200 to 300 cps. For devices of this nature, capacitors of proper size are currently available from the Integrated Circuit technology.

4.3 Darlington Amplifier

A thorough analysis of the Darlington configuration was made during this reporting period with special emphasis on the high frequency performance of the Darlington circuit. This curcuit, however, is of limited usefulness and, in almost all cases, the grounded emitter - grounded collector configurations are superior. The frequency response of the Darlington is approximately:

$$f = \frac{f_t}{\frac{2}{B}}$$

For the triple Darlington it is:

$$f = \frac{f_t}{\frac{3}{B}}$$

Thus for f_t = 300 mc and B = 30 for the triple Darlington

$$f = \frac{300}{(30)\quad(30)\quad(30)} = \frac{1}{90} \text{ mc} = .011 \text{ mc}$$

4.4. RF Amplifier

An analysis of the RF amplifier problem has been completed. It is apparent that no inductance will be required in the VHF receiver for gain purposes. The receiver selectivity will be obtained primarily by the use of 12 Mc crystal filters. The RC coupled amplifier design is based on the silicon NPN 2 N834 planned for integrated circuits.

4.5 VHF Receiver

During this period preliminary steps were taken toward the design of a V.H.F. Transceiver. The design will result in a working breadboard which will be used to evaluate circuits prior to and after Integrated Circuit implementation. Tentative block and Schematic diagram of the receiver portion, together with system specifications, were established.

The signal frequency for the transceiver has been set at 120 M.C. amplitude modulated. The receiver will be a fixed tuned, dual conversion system. The first I.F. center frequency will be 12.0 M.C. while the second I.F. will be 455 KC.

The receiver selectivity will be obtained through the use of two Crystal filters, one at 120 MC and one at 12.0 MC. The rejection of the image frequency is provided for by the 120 MC unit while the second Crystal Filter centered at 12.0 MC provides adjacent channel selectivity.

The use of Crystal Filters for the most part eliminates the need for large value inductors, especially at 455 KC. In addition, it is now possible to use RC coupled amplifiers to provide the necessary gain at both I.F. frequencies.

The local oscillators will be Crystal Controlled. The First L.O. will use a crystal operating on its fifth overtone to provide 108 MC, while the Second L.O. crystal will operate on its fundamental mode, i. e., 11.545 MC.

The remainder of the receiver, namely, the Audio Amplifier, First and Second Mixers, and A.G.C. Amplifiers will be of conventional design.

Figure 4.1 is a tentative block diagram for the receiver portion of the transceiver and Figure 4.2 is the schematic diagram. The specifications for the various functions are given below:

120 MC Crystal Filter

Center Frequency	120 MC
Gain	-12 db max.
$B.W._{3db}$	30 KC
Attentuation at Image (96 MC)	60 db
Z_i, Z_o	150 ohms

R.F. Amplifier

Center Frequency	120 MC
Gain	10 db
$B.W_{3db}$	50 MC
Z_i, Z_o	150 ohms

First Mixer — 120 Mc to 12 MC

Conversion Gain	10 db
Z_i at 120 MC	1000 ohms
Z_o at 12 MC	1200 ohms

First Local Oscillator

Frequency	108.0 Mc ± .005%
Frequency Drift	0.05 KC/°C

12 MC Crystal Filter

Center Frequency	12 Mc ± .01%
Gain	-12 db max.
B.W. 3db	18 KC
B.W. 60 db	100 KC

Minimum Attentuation Outside Pass Band 50 db

Maximum Variation of Attentuation

Over Passband	1 db
Z_i, Z_o	1200 ohms

12 MC I.F. Amplifier (RC Low Pass)

Gain	40 db
B.W. 3db	15 MC
Z_i	1200 ohms
Z_o	2200 ohms
AGC (AGC)	24 db

Second Mixer 12 MC to 455 KC

Gain	6.0 db
B. W. 3db	25 KC
Z_i at 12 Mc	1000 ohms
Z_o at 455 KC	2200 ohms

Second Local Oscillator

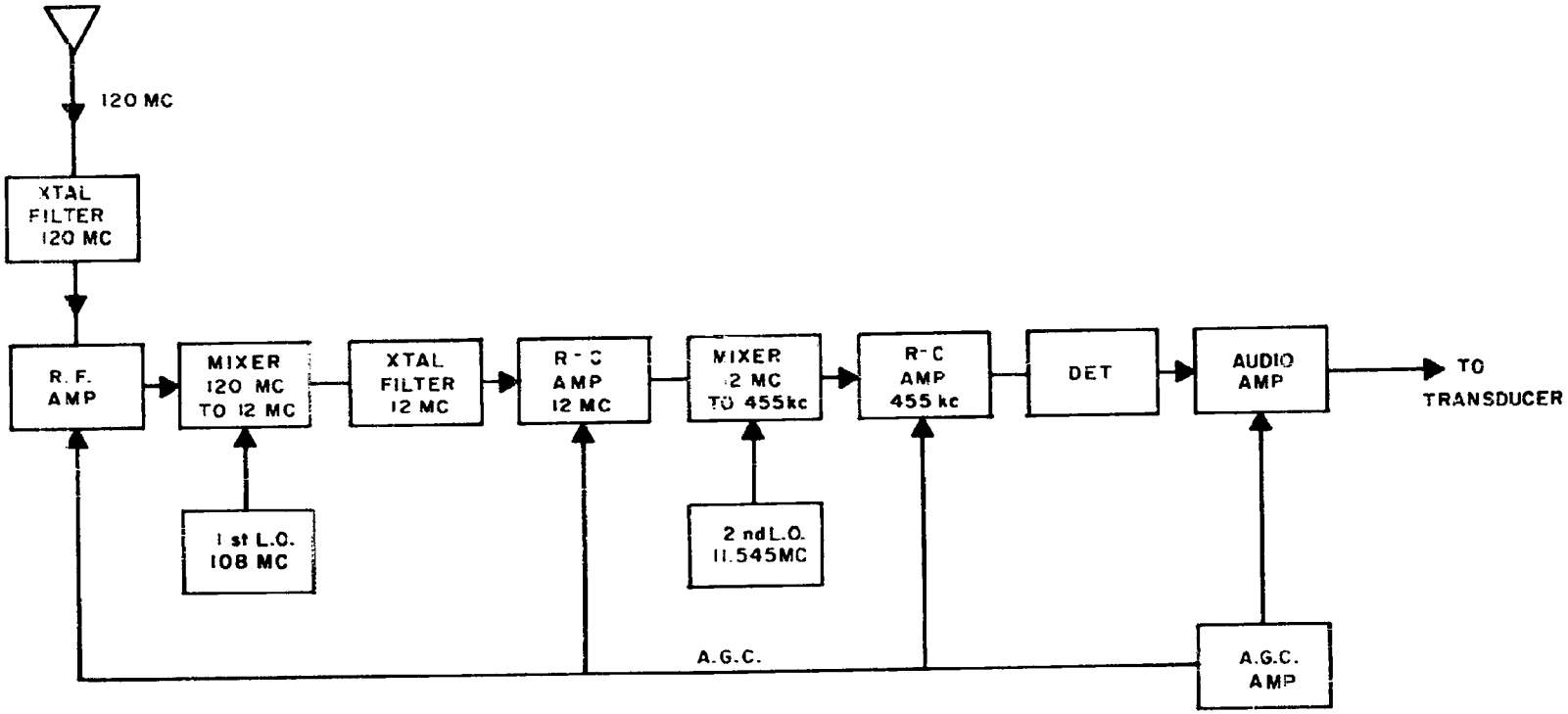
Frequency	11.45 MC + .005%
Frequency Drift	0.0054 KC/°C

455 KC I.F. Amplifier (R.C. Low Pass)

Gain	60 db
B.W. 3db	500 KC
Z_i	2000 ohms
Z_o	5000 ohms
AGC (AGC)	24 db

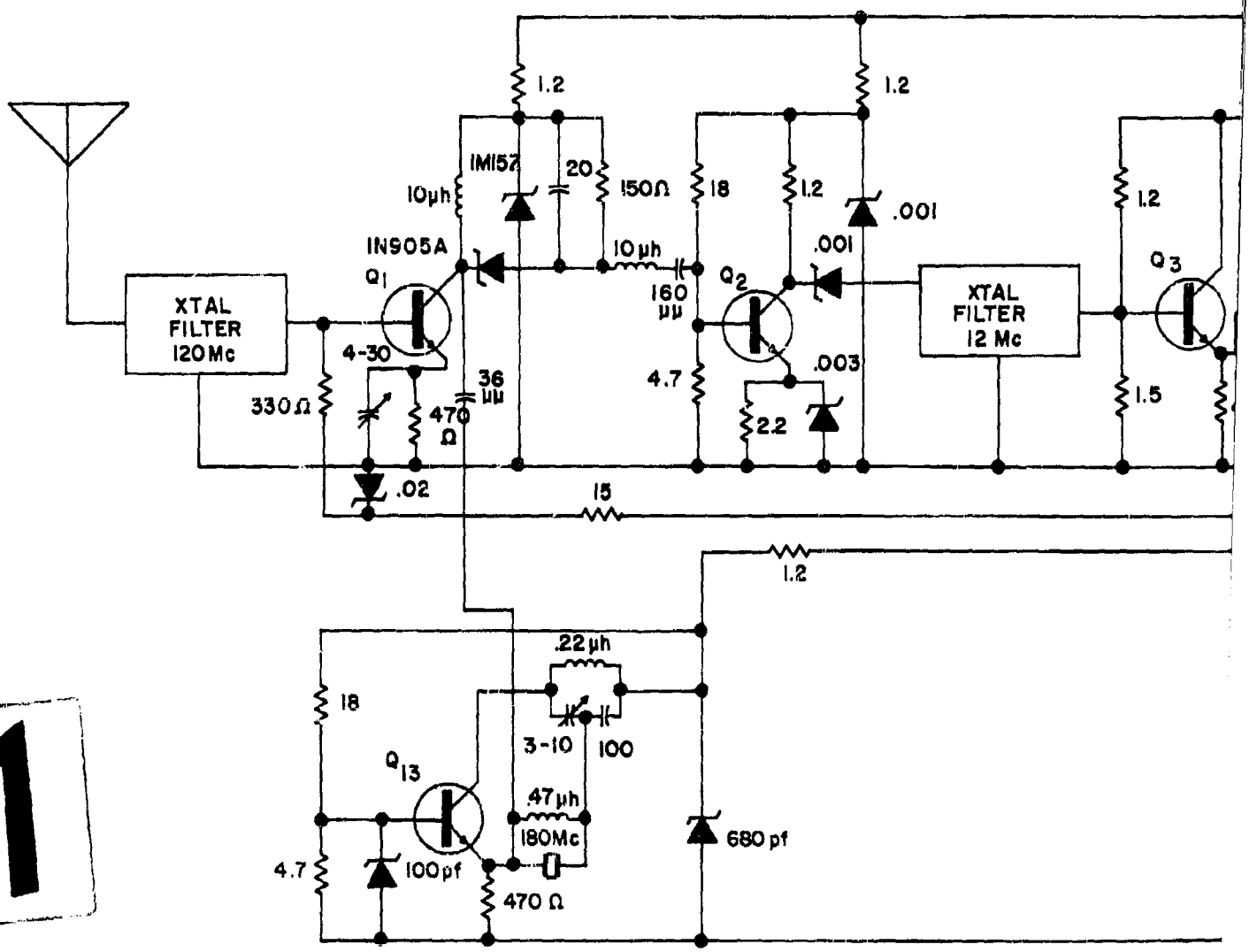
Detector & Audio Amplifier

Gain	40 db
B.W.	300 to 5000 cps
Output	10 MW
Z_o at 1000 cps	1000 ohms



RECEIVER BLOCK DIAGRAM

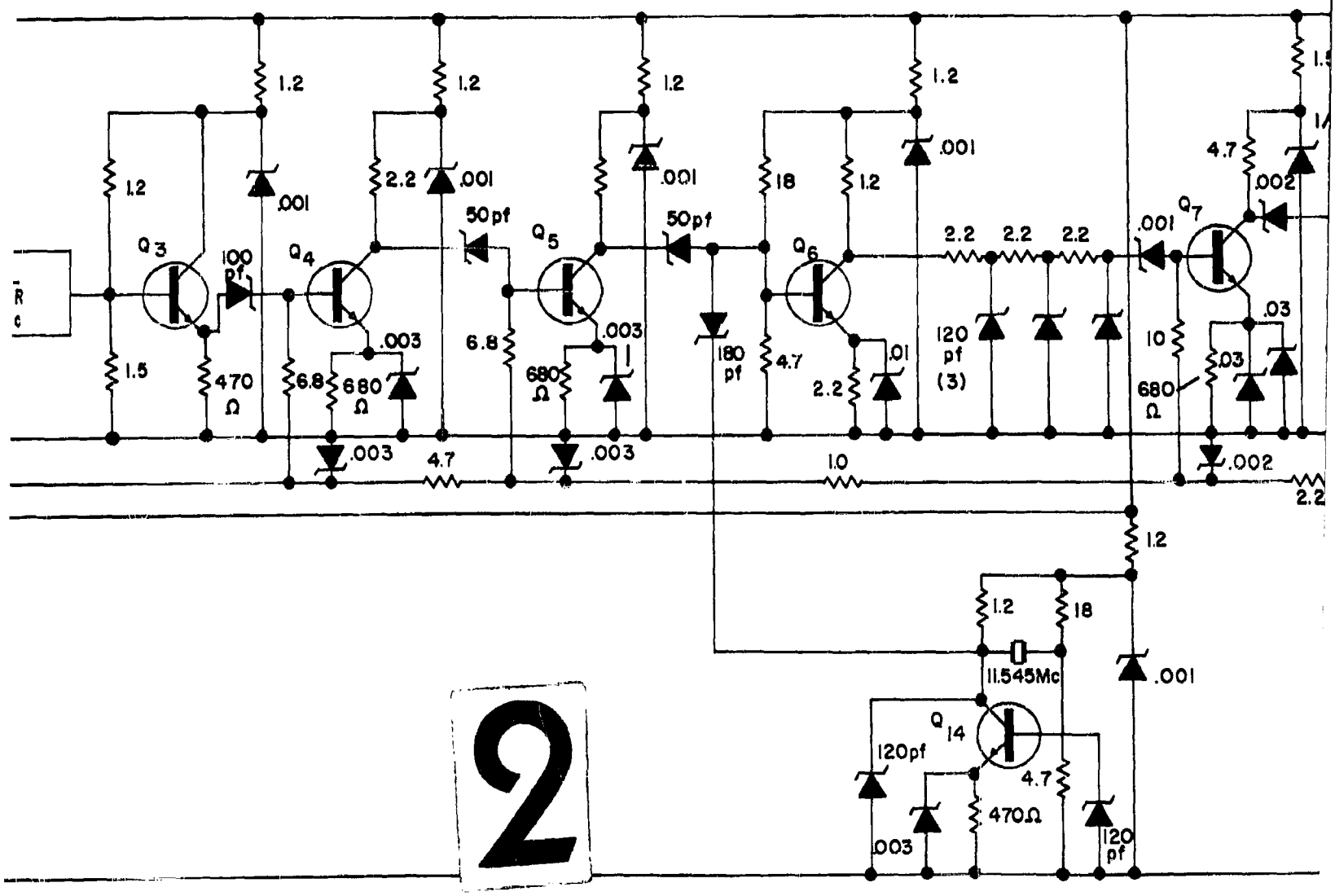
FIGURE 4.1



1

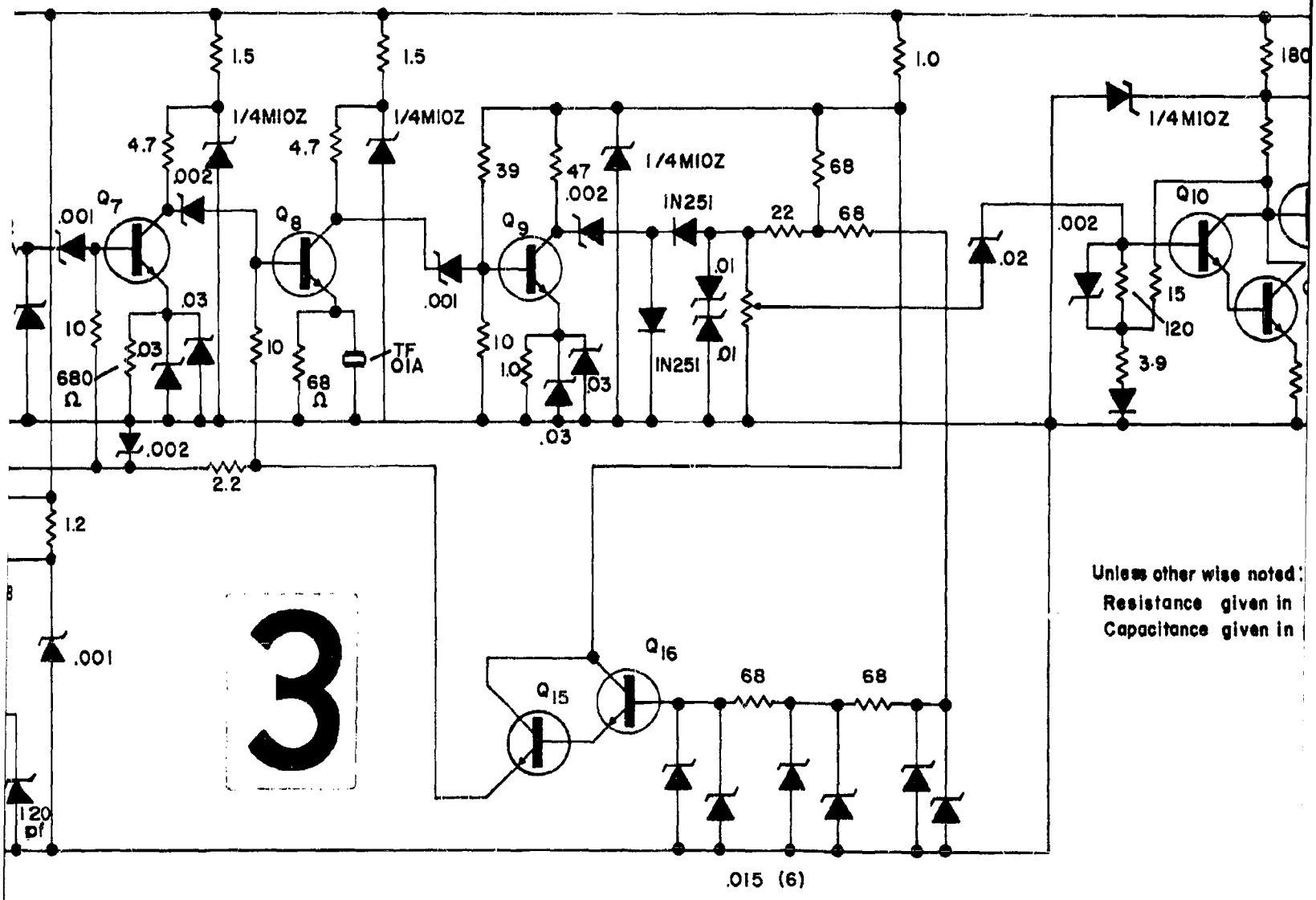
MOTOROLA Semiconductor Products Division

INTEGRATED CIRCUITS, RECEIVER SCHEMATIC (PRELIMIN

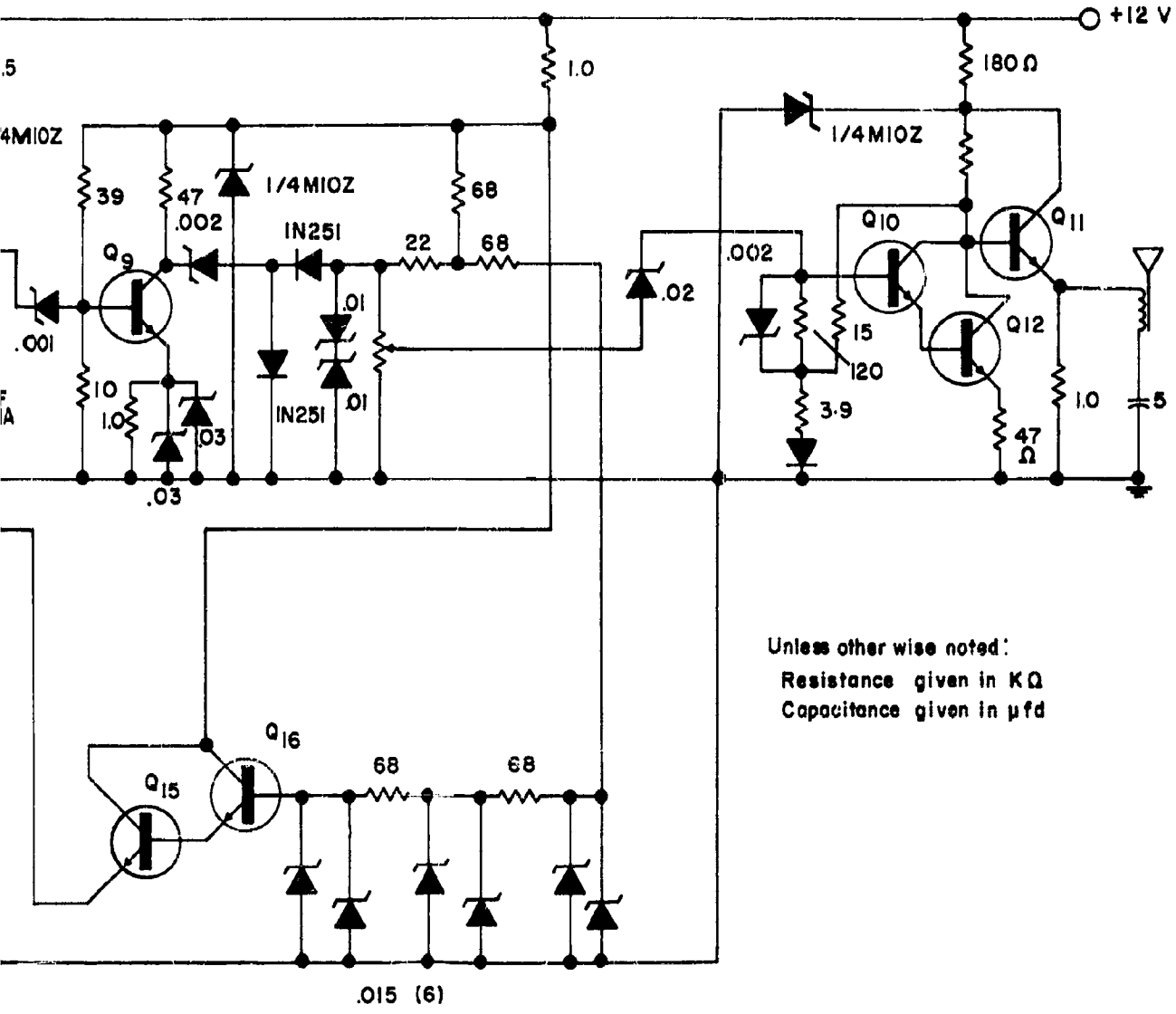


2

(PRELIMINARY)



3



Unless other wise noted:
Resistance given in KΩ
Capacitance given in μfd

Construction of the receiver breadboard was finished and, except for the 120 Mc Crystal Filter, the system is complete. Basically the breadboard performs as expected and only minor problems associated with the A.G.C. circuitry remain to be solved before system evaluation can begin.

One important feature of the breadboard is the inclusion of reversed-biased Zener diodes as capacitors. All capacitor functions of by-passing and coupling at frequencies up to and including 12 MC are performed by silicon capacitors.

Because of poor loss characteristics at high frequencies the silicon capacitors are not used in the 120 MC R.F. Amplifier or in the 108 MC First Local Oscillator.

The replacing of conventional capacitors with silicon capacitors is the first step toward providing a breadboard receiver system which is compatible with Integrated Circuit technology.

DISCUSSION OF CIRCUITRY

120 Mc Crystal Filter

The 120 MC Crystal Filter is the only component not included in the receiver breadboard. There are two approaches currently being followed in an attempt to relieve this situation. The first is to obtain crystals from a commercial manufacturer which have specified electrical parameters The present plan is to fabricate the crystals into a two-crystal balanced filter similar in topology to the type used for I.F.

Filters in communication receivers. It is not intended that this filter be of minimum size or conform to a particular shape. The main purpose is to obtain a specific characteristic at 120 MC as quickly as possible.

The other approach is being followed at Motorola's Chicago facilities. The goal of this program is to provide a filter which will be compatible physically as well as providing the specified responses. It is expected that this work will be completed January, 1962.

R.F. Amplifier

The R.F. Amplifier used in the breadboard is referred to as an R-F Amplifier and provides 12 db voltage gain. The variable capacitor in the emitter circuit is tuned to resonate with the emitter lead inductance at 120 Mc. The amplifier is a very broad band device having a band width 50% to 60% of the center frequency.

108 MC Local Oscillator

The first local oscillator is a crystal-controlled Colpitts circuit. The active element is connected in a common base configuration with silicon capacitors serving as R.F. by-passes. The crystal proper is operated at its fifth harmonic in the series resonant mode providing a low impedance feedback path from collector to emitter at 108 MC. To insure operation at the fifth overtone, the collector

circuit is tuned to the LO frequency. The output is taken from the emitter to provide a low source impedance for injection into the 150 ohm first Mixer circuit.

First Mixer

The first Mixer in the receiver breadboard is a IN905 planar diode operating at the R.F. amplifier collector potential. Oscillator injection occurs at the collector with the Mixer providing the proper R.F. amplifier load. The crystal is operated at approximately 0.7 ma rectified D.C. current; a level which gives favorable conversion loss and noise figure.

Crystal Filter Driver

The Crystal Filter driver provides broadband amplification around 12 MC and a constant generator impedance for the 12 MC Crystal Filter. Coupling from the mixer is through a series resonant circuit tuned to 12 MC. This same circuit isolates the Filter Driver from the R.F. Amplifier and the 108 MC oscillator. The Filter Driver is a common emitter amplifier utilizing silicon capacitors for by-pass and decoupling 12 MC I.F. Amplifier.

12 MC I.F. Amplifier

The 12 MC I.F. Amplifier consists of an emitter follower Crystal Filter load followed by two common emitter R-C Amplifier stages. The emitter follower provides a constant load impedance for the Crystal Filter as well as power gain.

Silicon capacitors are used for decoupling of the collector supply as well as interstage coupling to the I.F. Amplifier. A.G.C. is not applied to this stage in order to maintain a nearly constant input impedance.

The two stage common emitter amplifier is a broad-band device. The upper cut-off frequency is determined by the transistor used while the low frequency cut-off is primarily determined by the value of interstage coupling capacitor. The gain of both stages is determined by the A.G.C. level present.

11.545 MC Oscillator

The Second Local Oscillator is a crystal controlled Pierce Oscillator. Contrasted with the First LO, the Second LO does not contain any frequency determining elements other than the crystal itself. The crystal operates in the antiresonant mode providing feedback from collector to base. Output is taken from the collector for injection into the Second Mixer stage.

Second Mixer

The second mixer combines the signals from the 12 MC Amplifier and the 11.545 MC Second LO to form the 455KC Second I.F. frequency. In addition, the Second Mixer is active in that the stage provides voltage gain. Circuit wise the Mixer-Amplifier is a common emitter similar to the 12 MC I.F. Amplifier. The output of the Mixer is connected to a

3-section R.C. low-pass filter. The corner frequency of the filter is set at 50(KC.

455 KC I.F.

The 455 KC I.F. Amplifier is a 3-stage common emitter R.C. Amplifier. Gain control for the Amplifier is provided for by application of A.G. C.Voltage to the first two stages A series resonant ceramic piezoelectric filter tuned to 455 KC is used as an emitter by-pass in the second stage. The filter provides a degree of selectivity which reduces the level of the Second Local Oscillator signal.

Demodulator

The Demodulator consists of a diode voltage-doubler type detector plus associated silicon by-pass and coupling capacitors. A small current from the A.V. C. Amplifier bias circuit minimizes the effect of the diode offset voltage by keeping both diodes baised "on" with on signal present.

A.V.C. Amplifier

The A.V.C. Amplifier consists of a Low pass R-C filter and a Darlington type current amplifier. The R-C filter removes the higher frequency audio components from the A.V.C. Voltage. A Darlington amplifier is necessary to transform the required high filter impedance to a low source

impedance which can supply the base current for the R.F. and I.F. Amplifier stages.

Audio Amplifier

A two stage Darlington connected as a common emitter voltage amplifier plus a direct coupled emitter follower comprise the Audio Amplifier. The Darlington connection provides a high input impedance so that adequate low frequency response is obtained. The forward biased diode in the base bias circuit of the input transistor provides a degree of V_{BE} compensation. The subminiature speaker is driven by the emitter follower. The speaker being used in the breadboard requires D.C. isolation, therefore, the large value capacitor. Alternate approaches are being considered in an attempt to eliminate the need for the capacitor.

Forecast

Work during the next period will be divided into two inter-related tasks. The first is the evaluation of the receiver breadboard to determine items such as system sensitivity, bandwidth, A.G.C. characteristics and noise figures.

In addition, discrete integrated circuit components will become available for evaluation and inclusion into the breadboard. What, if any, effect the new components will have on system performance will have to be determined.

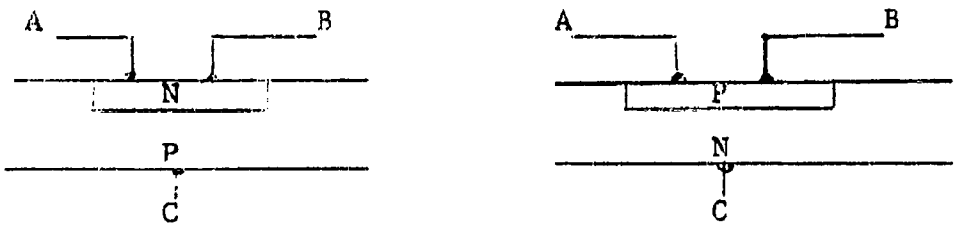
5. INTEGRATED CIRCUIT TECHNOLOGY

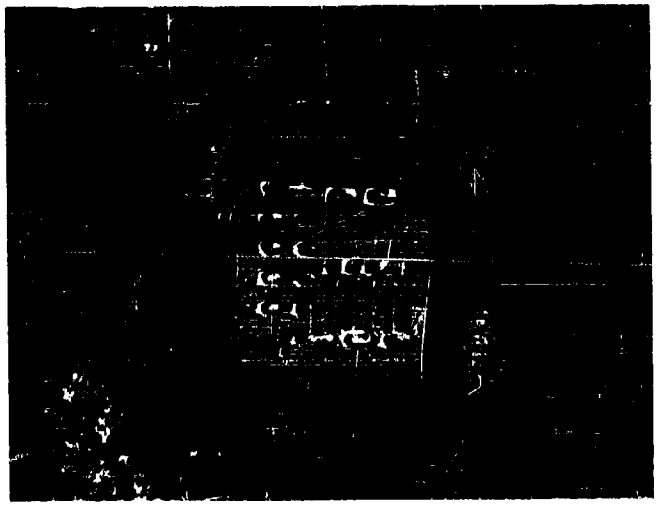
The passivated-planar-epitaxial process appears to offer the best basis for integrated circuit technology at the present time. The planar passivation process provides a flat compatible substrate for thin film deposition. During this period, in addition to continuing improvement in transistor and diode fabrication, a number of compatible components have been developed.

5.1 Compatible Diffused Resistors

The diffused resistor is a "natural" integrated circuit component. The base diffusion for some silicon transistors is normally in the range of 100 to 400 ohms per square. Thus this diffusion easily covers resistor values to 30 K. A picture of the segmented diffused planar passivated resistor is shown in figure 5 1. The emitter diffusion may also be used to provide resistors with the heavier doping required for emitter injection efficiency. The resistance values are lower than those obtained from base diffusion.

The diffused resistor may be most simply characterized as extended r_b [1] The fabrication process either diffuses N into P material or P into N.



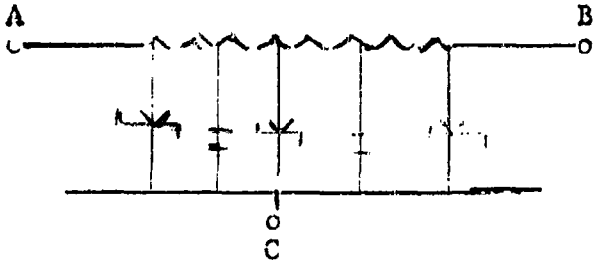


SEGMENTED DIFFUSED
PLANAR PASSIVATED RESISTOR

FIGURE 5.1

The resistance appears between points A and B, which are ohmic contacts. The power dissipation of the diffused resistor depends on the area used and the substrate temperature. The power dissipation will range from 10 mW to 250 mW in practical integrated circuits.

The equivalent circuit for the diffused resistor is shown below.



The circuit shown is the P diffused into N. The breakdown voltage of the diodes is determined by the higher of the two resistivities used for the N and P layers.

It is obvious from the equivalent circuit that the bias applied to C is important. It must be positive with respect to points A and B or left open.

The capacity of the 110 square variable value diffused resistor to the substrate is about 5 pf. The resistor value is approximately 30 K ohms, for a 300 ohms/ square diffusion.

The diffused resistor has a better temperature coefficient than that of a shaped, high resistivity silicon resistor, which is about ± .8% per ^{o}C in the practically usable

range, It is also fabricated by photolithography rather than by mechanical techniques. The temperature coefficient of a typical diffused resistor is shown in Figure 5.2. This temperature coefficient is for 300 ohms per square. Heavier doping would reduce this coefficient. A substantial number of these units are being fabricated for reliability studies and further electrical evaluation, including manufacturing tolerances. Uniformity of resistance is indicated in Figure 5.3 where a cumulative plot of resistance for each segment is shown.

5.2. Compatible Silicon Dioxide Capacitors

Considerable numbers of capacitors were fabricated using thermally grown silicon dioxide dielectric on low resistivity N type silicon. Figures 5.4 and 5.5 show the distribution of capacity as well as the equivalent parallel resistance at 100 Hc. These capacitors have 36 mil diameter of aluminum and the thickness of the dielectric is approximately 1000 angstroms.

6.0 Fabrication

6.1 Circuit Isolation

The present scheme for electrical isolation in mock-up circuits of compatible components consists of individual chips mounted on a selectively metallized ceramic disk. All electrical interconnections are formed by thermo-compression bonding,

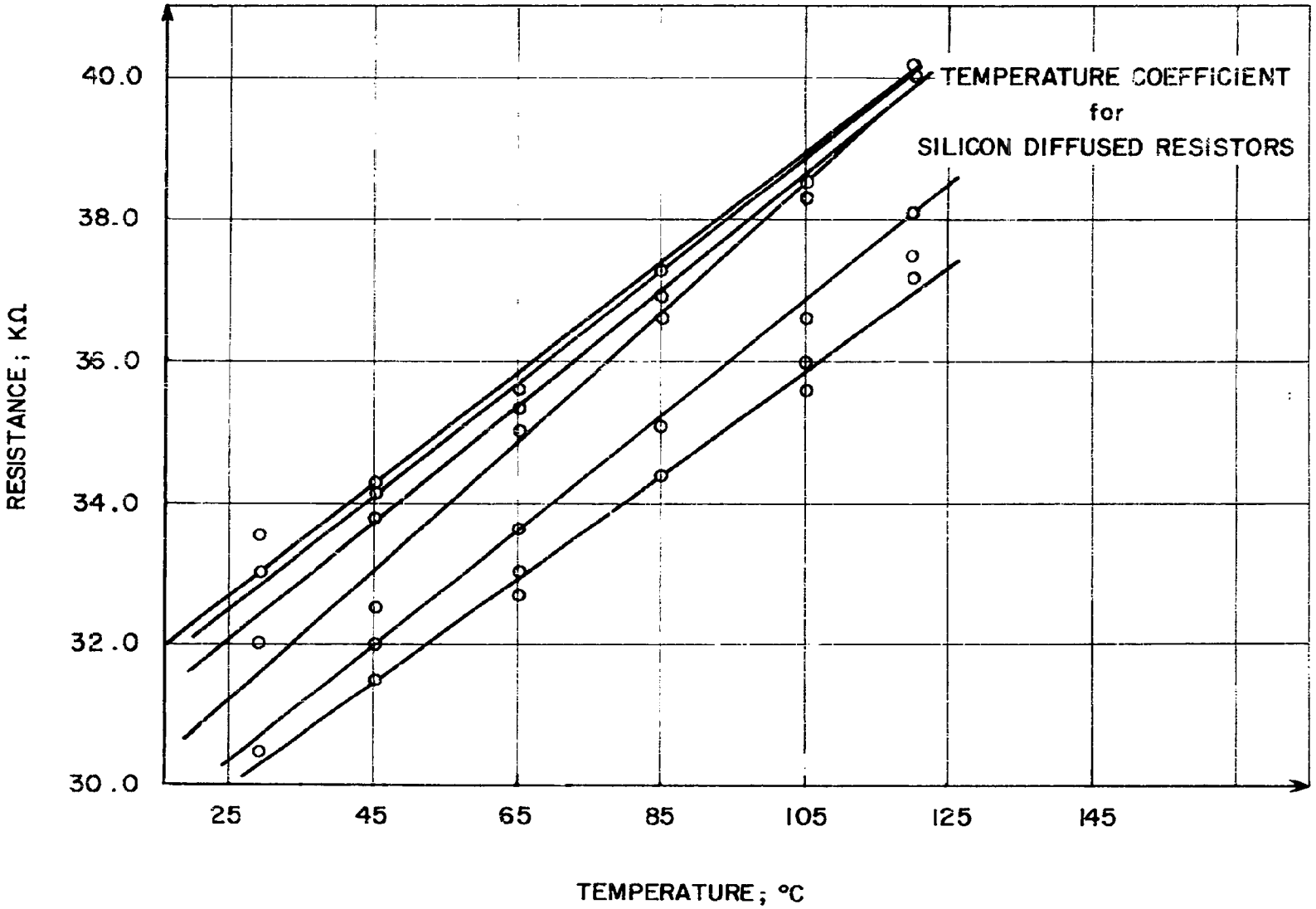

TEMPERATURE COEFFICIENT
for
SILICON DIFFUSED RESISTORS
RESISTANCE; KΩ
40.0
38.0
36.0
34.0
32.0
30.0
25
45
65
85
105
125
145
TEMPERATURE; °C

FIGURE 5.2

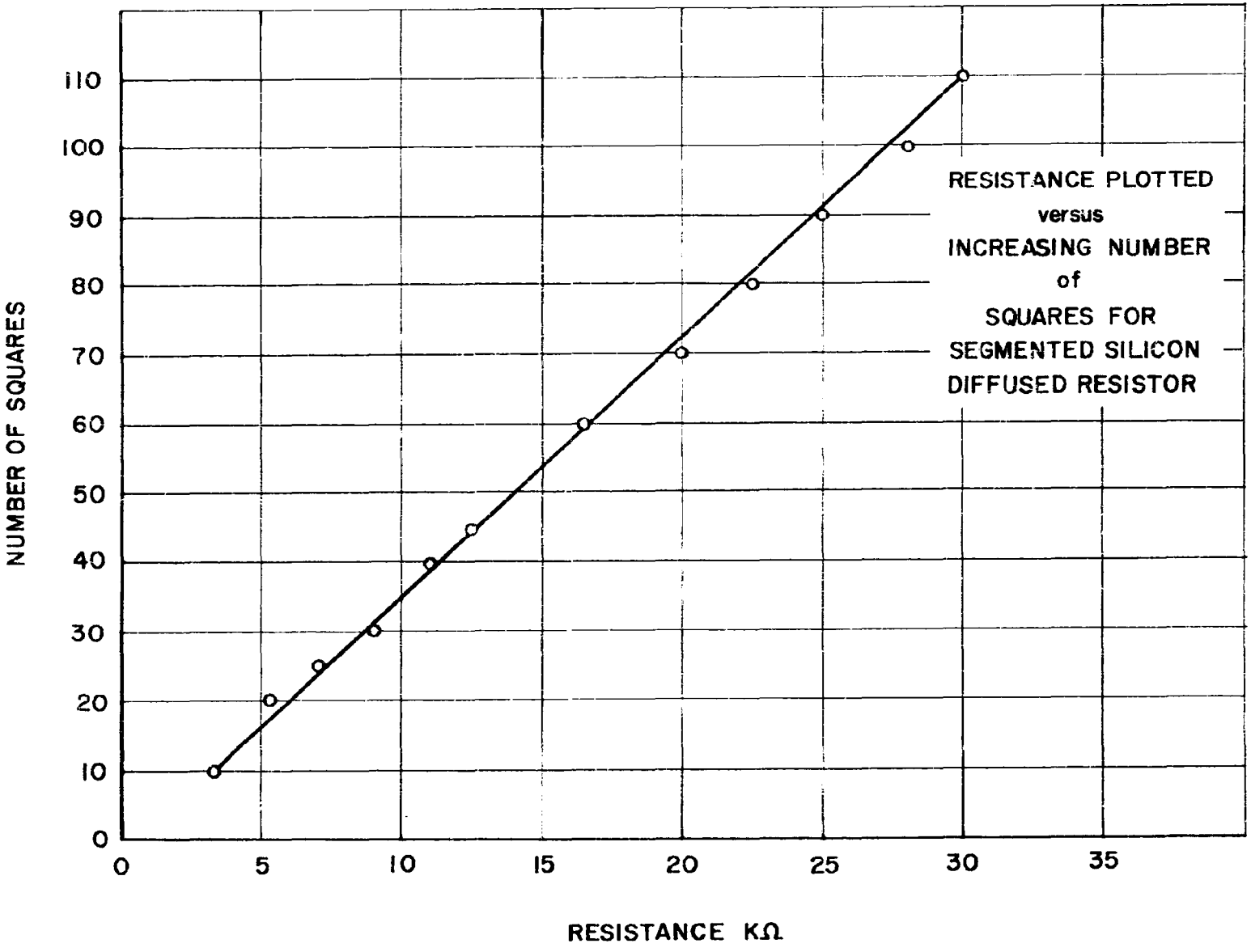

NUMBER OF SQUARES
110
100
90
80
70
60
50
40
30
20
10
0
0
5
10
15
20
25
30
35
RESISTANCE KΩ
RESISTANCE PLOTTED
versus
INCREASING NUMBER
of
SQUARES FOR
SEGMENTED SILICON
DIFFUSED RESISTOR

FIGURE 5. 3

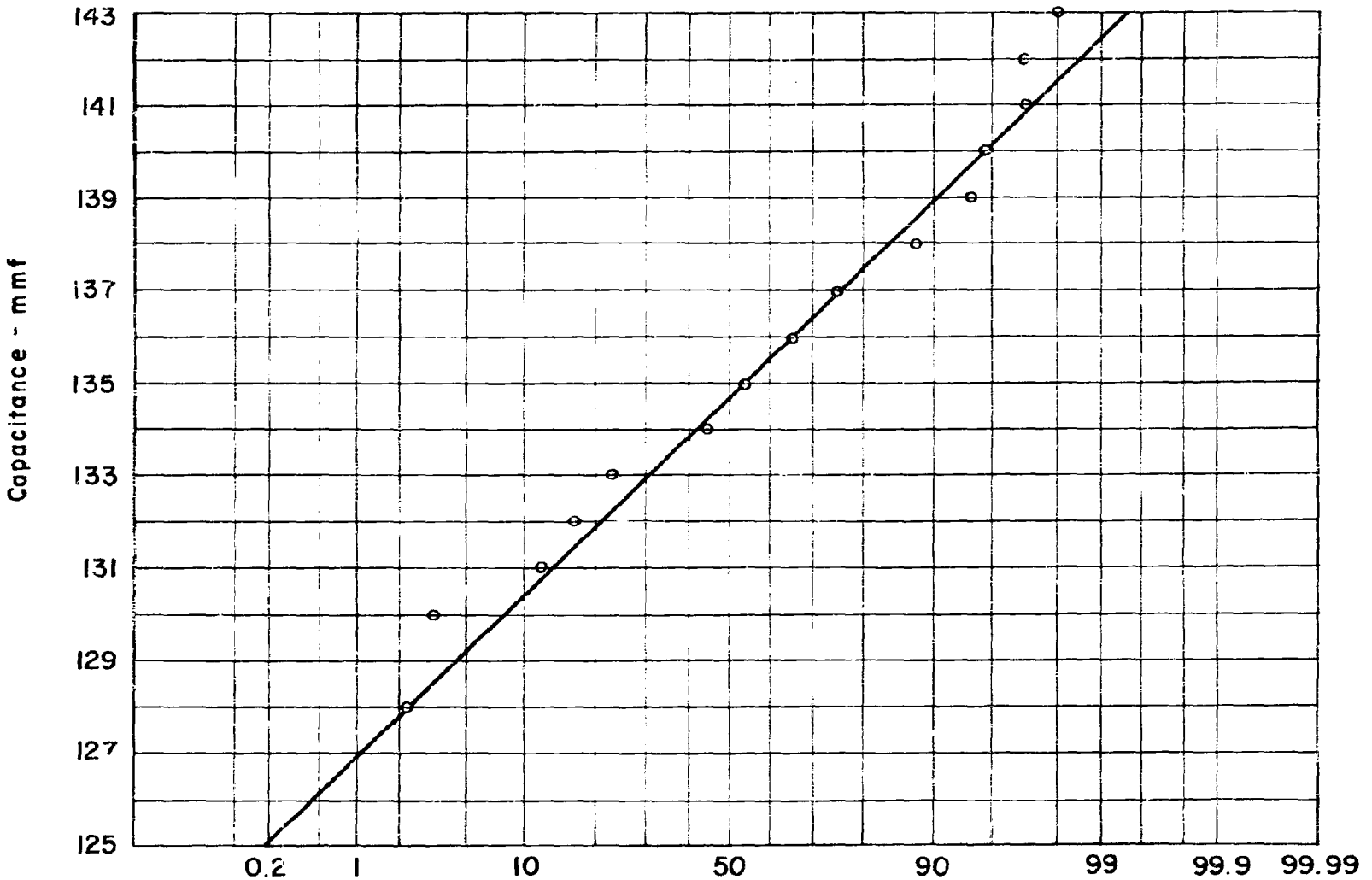

Capacitance - mmf
143
141
139
137
135
133
131
129
127
125
0.2
1
10
50
90
99
99.9
99.99

FIGURE 5.4

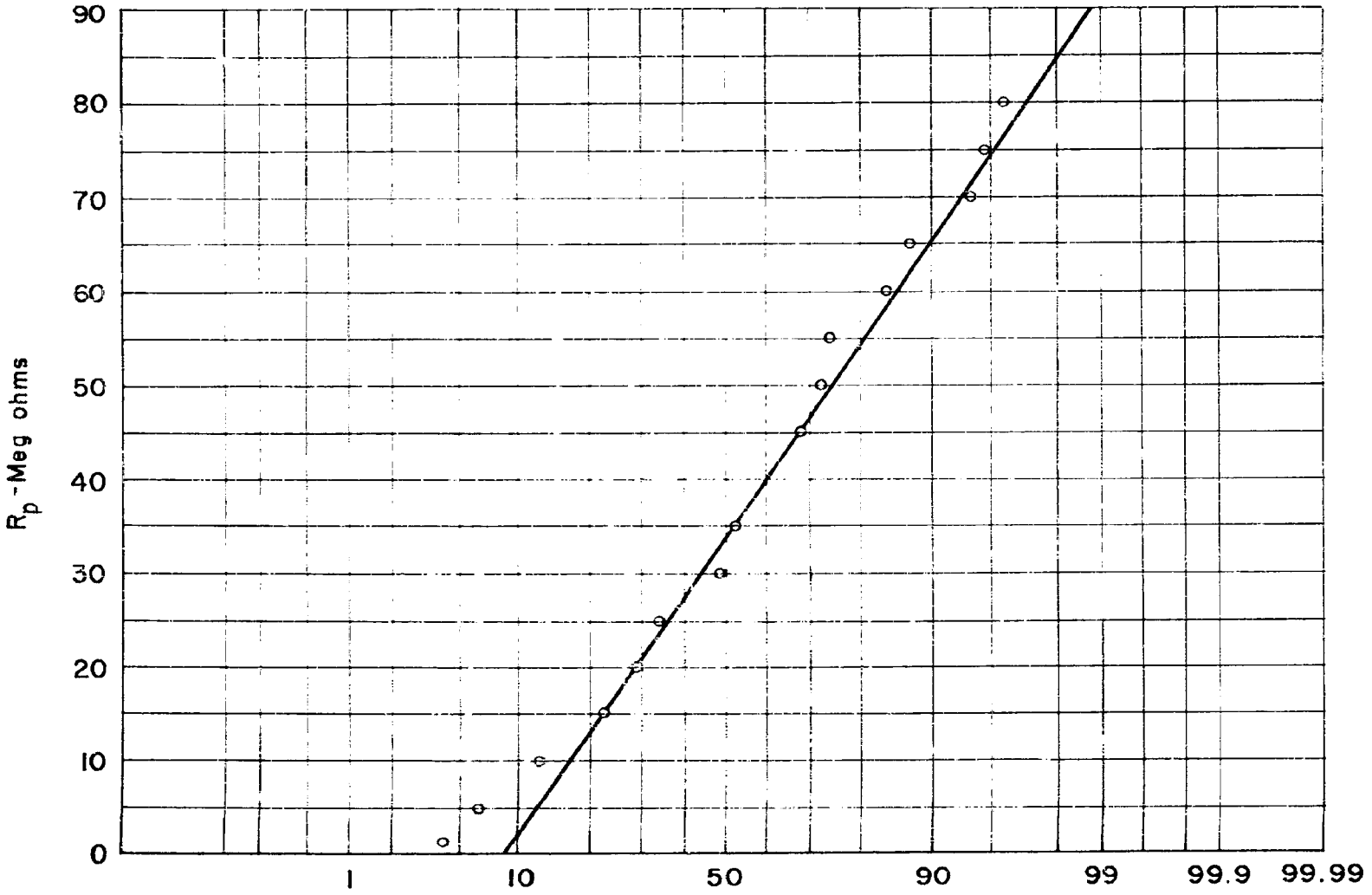


FIGURE 5.5

fine wires, from structure to structure. A method is being investigated for isolating structures on a single slab of silicon. This technique involves triple diffusion, in which N-type planar collector regions are formed in high resistivity P-type silicon. In order to evaluate this system and its effectiveness, a building block of two transistors and two resistors has been designed. These structures will be electrically isolated from each other, and electrical interconnections may initially be made by thermo-compression bonding. This initial building block will be an ideal element for the study of parasitics, since the resistors may be used as either resistors, capacitors (reversed-biased junctions), or as diodes. Also, this element may be used as a fundamental building block for evaluating various types of circuits. Such a fundamental block may be used to perform any number of circuit functions, and an evaluation of a circuit may be performed and adjustments made in the circuit prior to designing a masking set. One of the more useful functions of this block will be to evaluate various schemes of interconnection by selective metallization. All contacts, including collectors, will be brought to the surface so that any conceivable interconnection pattern may be employed.

6.2 Fabrication Facilities

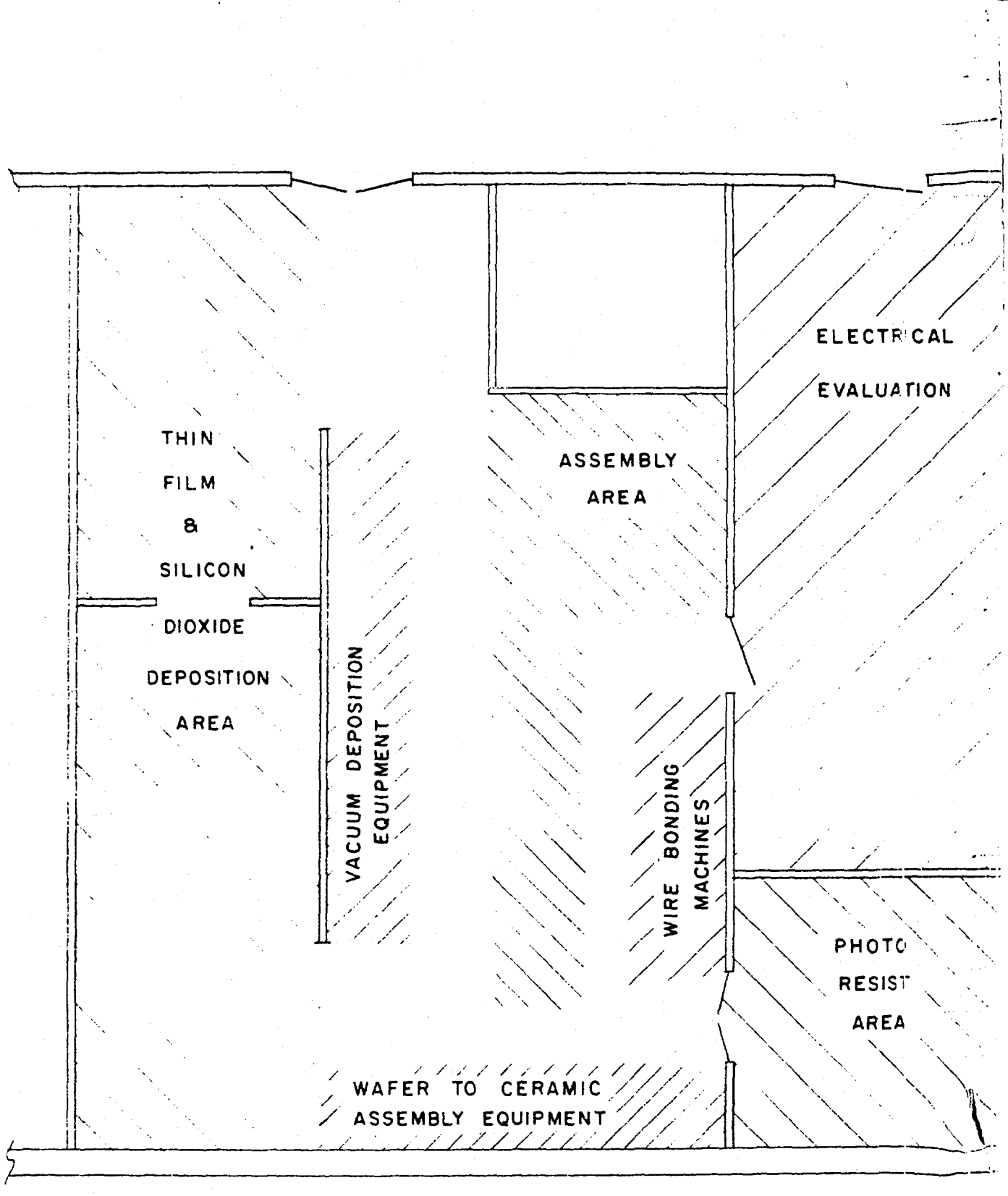
The construction of the Integrated Circuit Laboratory

See Figure 6.1 is in the final stages of completion. This room has humidity and dust control. Circulating the entire room are twelve types of water and gas services. There are hydrogen, oxygen, argon, nitrogen, forming gas, natural gas, vacuum, dry air, compressed air, deionized water, soft water, and raw water.

A great deal of the specialized equipment has been constructed and placed in operation.

6. 3 Packaging

The TO-5 and TO-18 headers have been used to package integrated circuit elements for test purposes. A final packaging method will be developed later in the contract period so the full benefits of process studies, as well as the results of the surface passivation work, are completed.



INTERGRATED CIRCUIT LAB

FIGURE 6.1

UNCLASSIFIED